

Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ixex Peak-M

2010-01-18

REV : X-build

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>



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```
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom
```

Clock Generator
SLG8SP585

100MHz/
2.5Gbps
PCle x 16
Bandwidth
: 8GB

Intel CPU

Arrandale

8,9,10,11,12,13,14

DMIx4	FDI (UMA)
2.5 GT/s	2.7 GT/s

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIe ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE

The diagram shows a block representing the **NUVOTON NPCE781BA0DX** microcontroller. It has three external components connected to it:

- Flash ROM 256kB**: Connected via an **SPI** interface (indicated by a single-headed arrow pointing from the microcontroller to the ROM).
- Touch PAD**: Connected via an **I2C** interface (indicated by a double-headed arrow).
- Int. KB**: Connected via an **I2C** interface (indicated by a double-headed arrow).

Each of the two I2C-connected components (Touch PAD and Int. KB) is labeled with a **68** in the bottom right corner, likely representing a pin count.

Project code : 91.4ES01.001
Part Number : 48.4ES11.0SB
PCB P/N : 09297
Revision : SA

Power SW
TPS2231R

New Card
(On daughter board)

PCIE x 1 → **10/100/1000LOM**
RTL8111DL 35
(On daughter board)

RJ45
CONN 61

Mini-Card
802.11a/b/g/n 65

Mini-Card WWAN/ WiMAX	64
--	----

USB 2.0 x 1

*Touch Panel
(only for 15'')*

USB 2.0 x 2

USB 2.0 x 1

Right Side:
USB x 1

USB 2.0 x 1

USB 2.0 x 1 *Bluetooth*

USB 2.0 x 1

Biometric

**Thermal
& Fan**
EMC2102 39,58

Capacity Board
(On daughter board)

CPU DC/DC
ISL62883 ^{47,48}

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC
TPS51125 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC
TPS51116 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC
ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC
TPS51218 86

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER
BQ24745

INPUTS	OUTPUTS
+DC_IN	+PWR_SRC

SYSTEM DC/DC
TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	VTT_CORE

LDO
APL5930

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO
RT9025 87

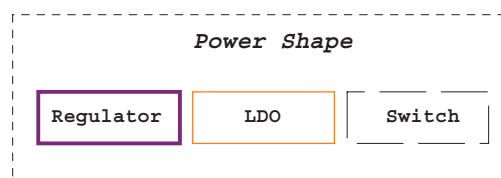
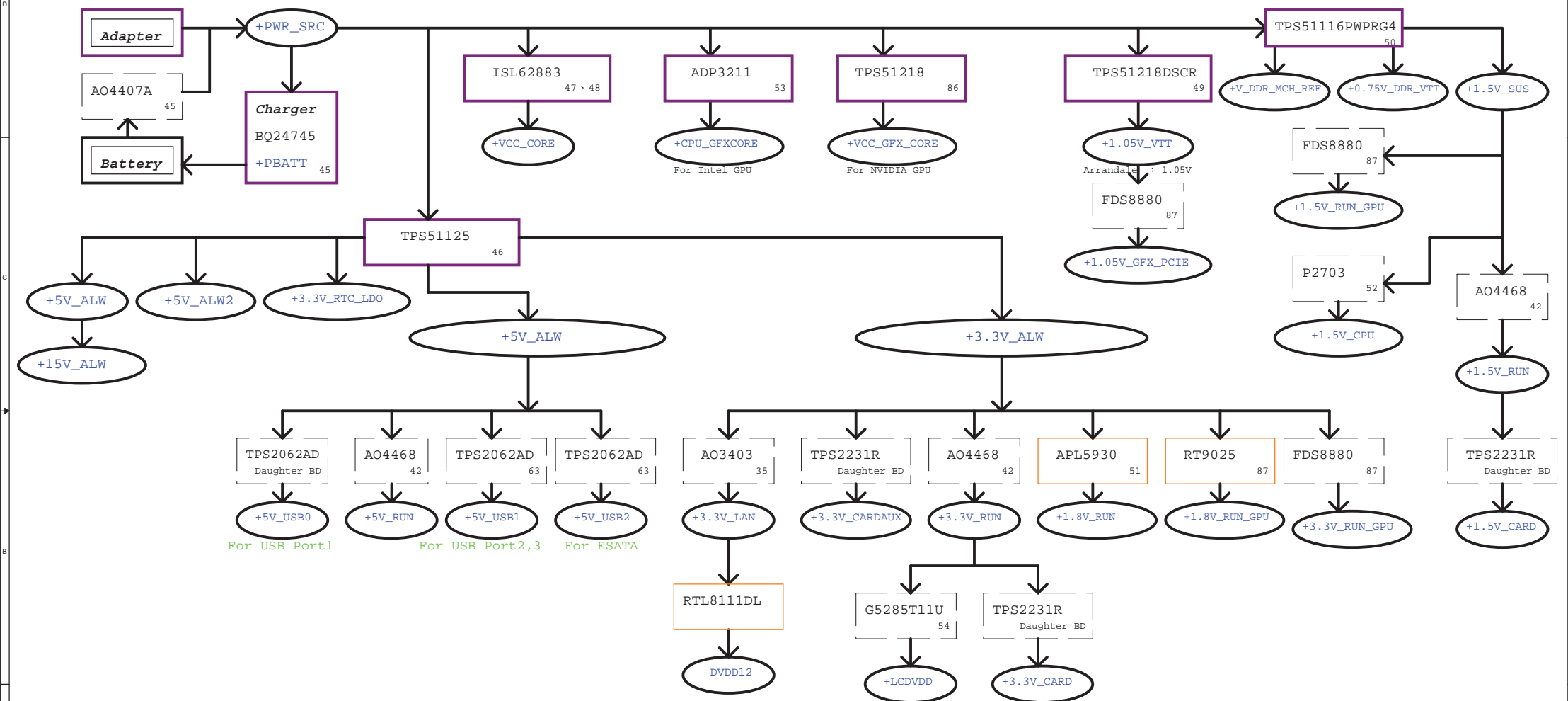
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DELL

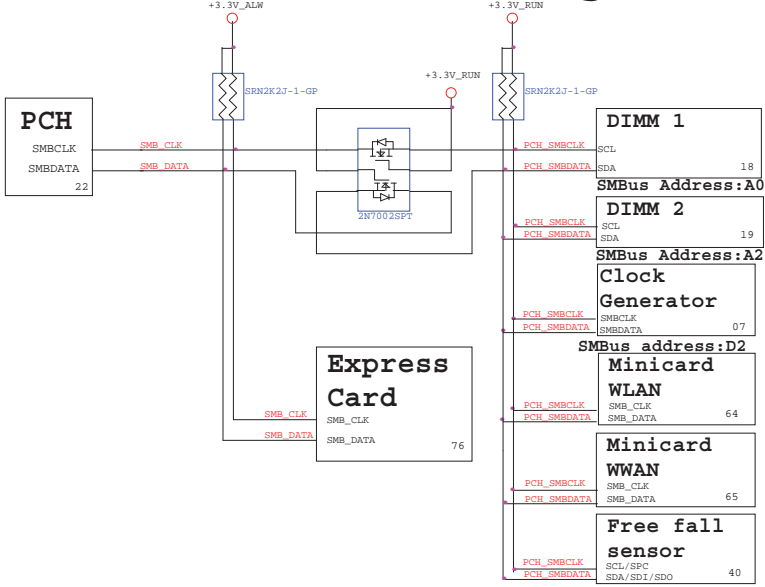
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Block Diagram

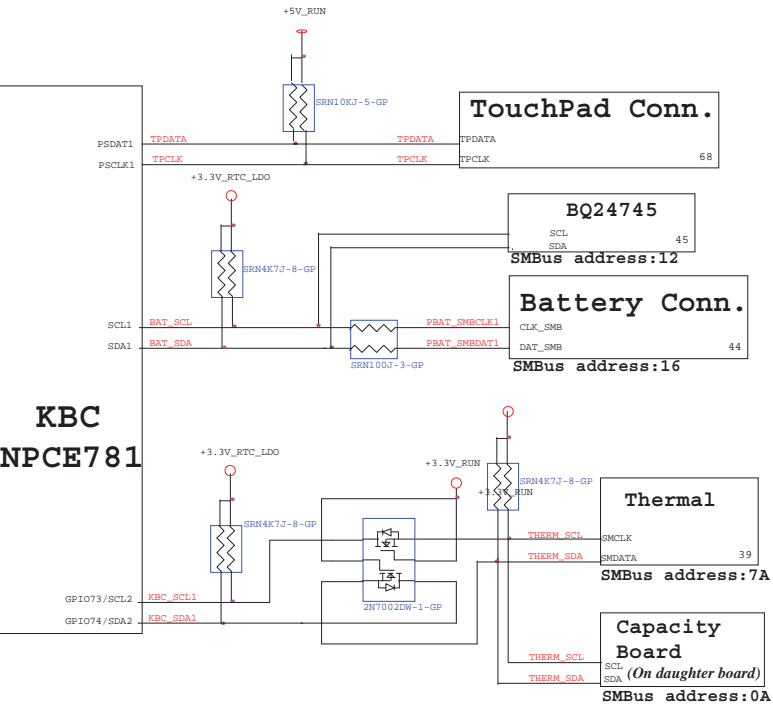
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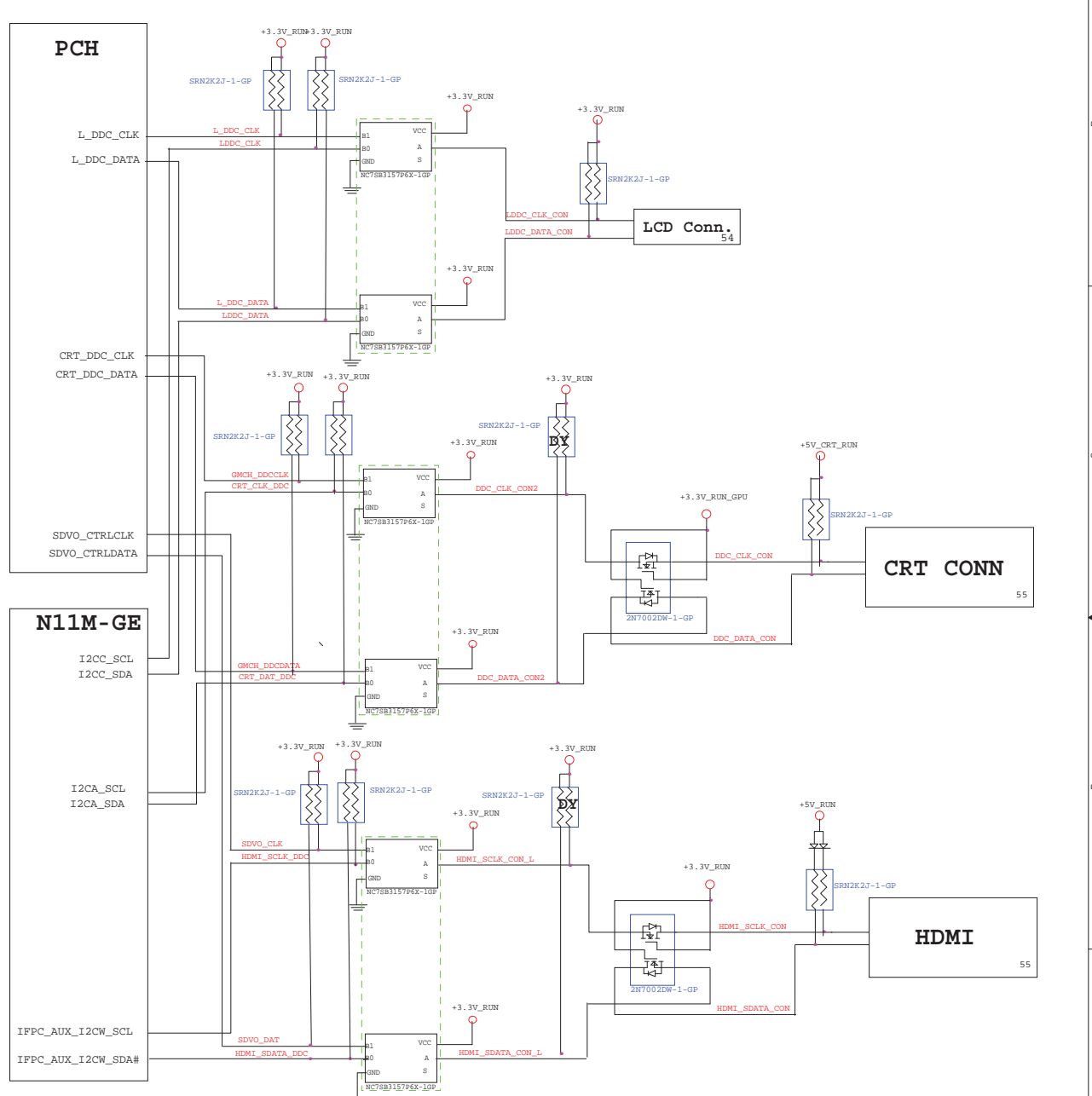
PCH SMBus Block Diagram



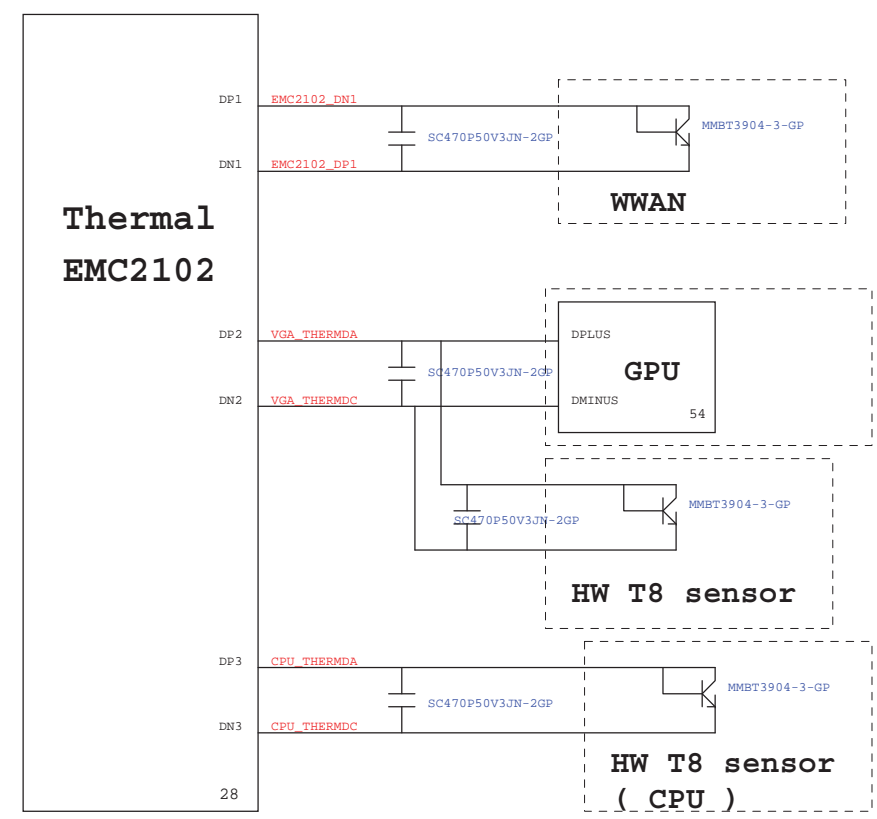
KBC SMBus Block Diagram



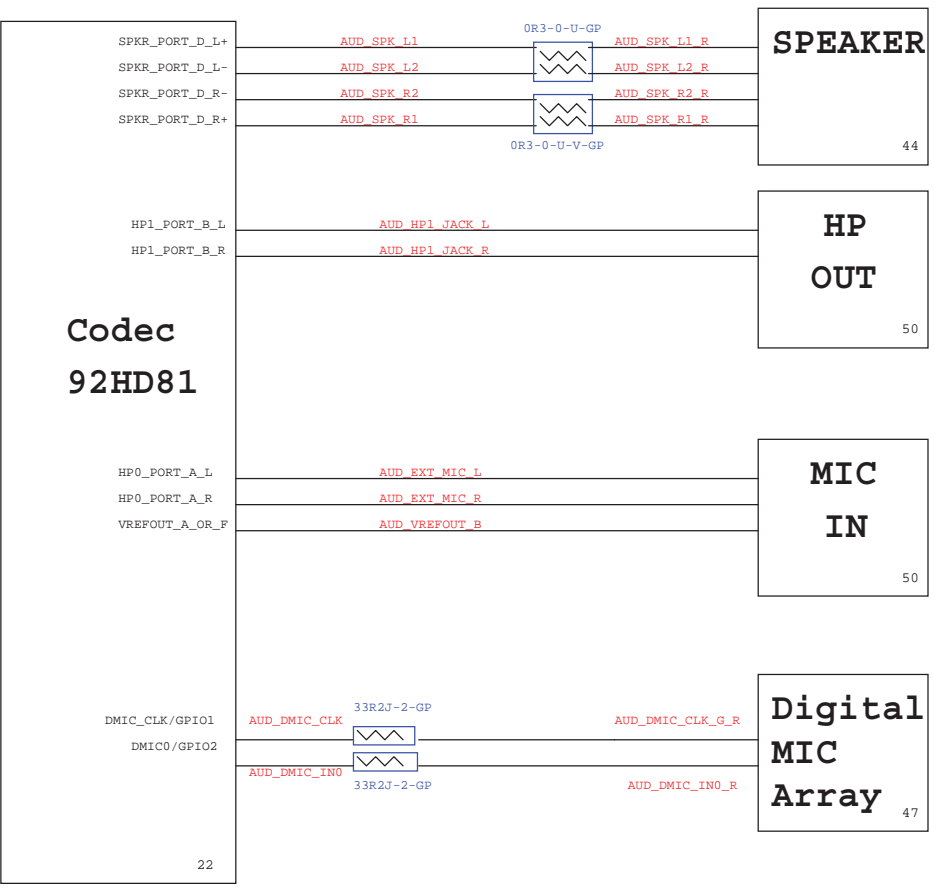
Switchable Graphic SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap ModeNote: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 k do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

Processor Strapping

Calpella Schematic Checklist Rev.0_7

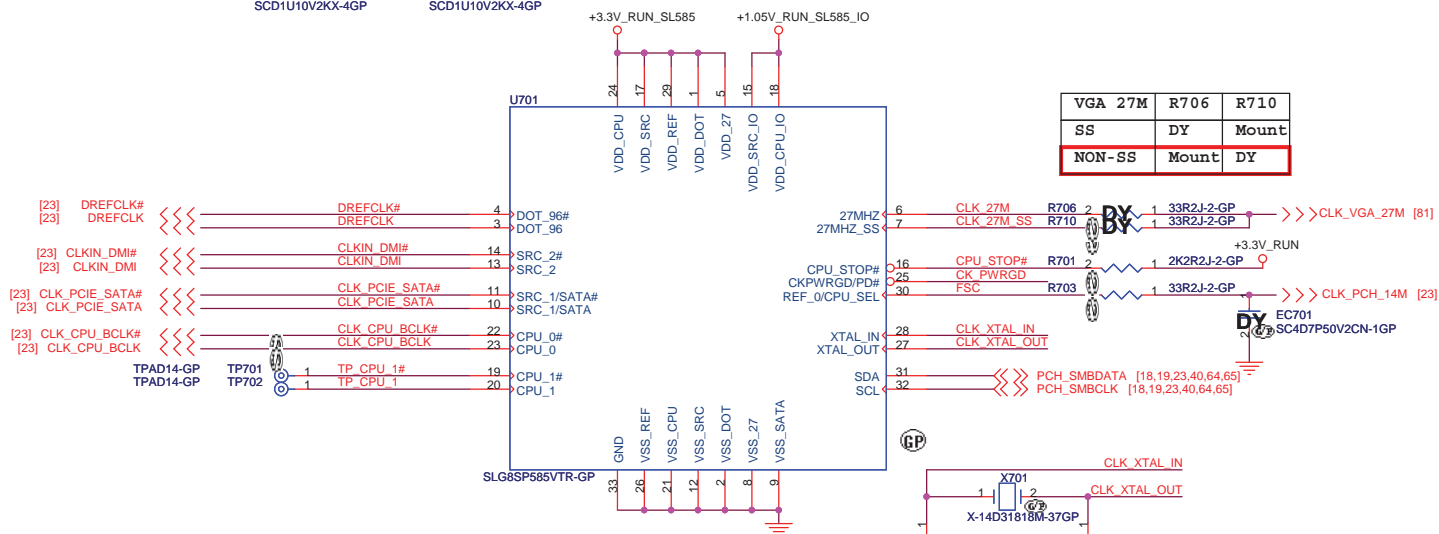
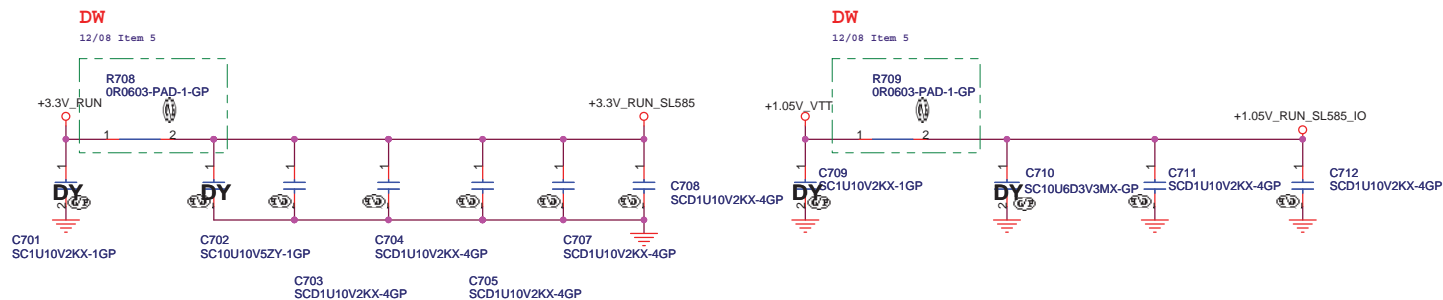
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

<Core Design>

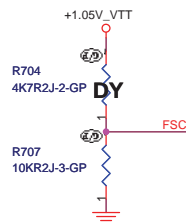


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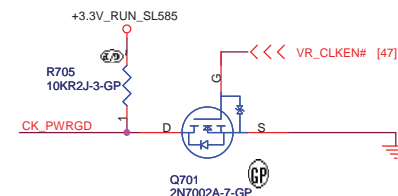


1st Silego 71.08585.003
2nd ICS 71.93197.003



VGA_27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY

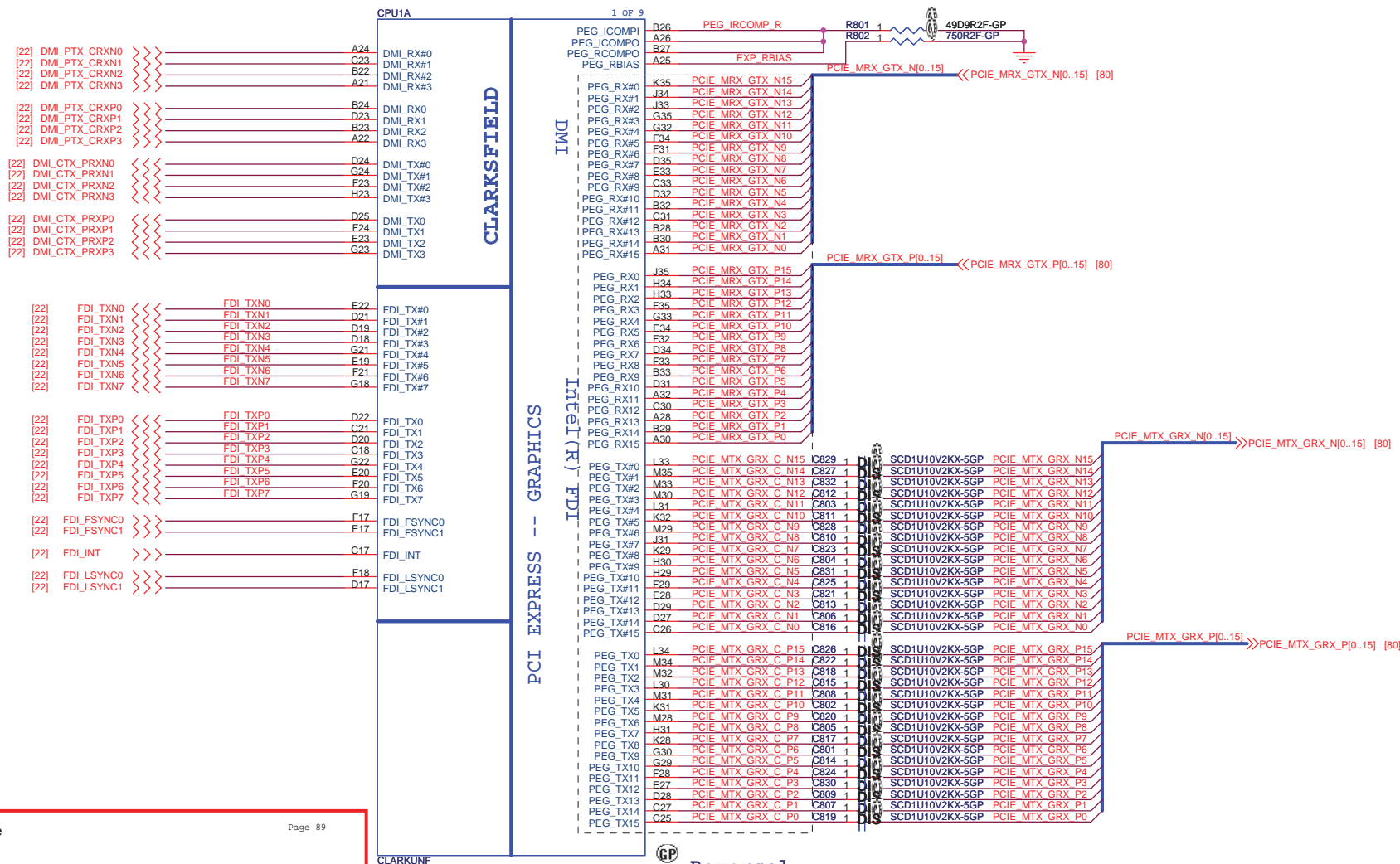
FSC	0	1
SPEED	133MHz (Default)	100MHz



<Core Design>



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Clock Generator SLG8SP585		
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Calpella Platform Design Guide Revision 1.6

2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarkfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX# [7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

Reversal

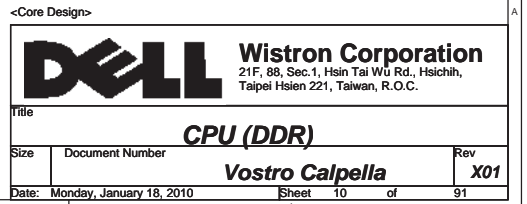
1. PCI-Express Static Lane Reversal
(15 -> 0, 14 -> 1, ...)

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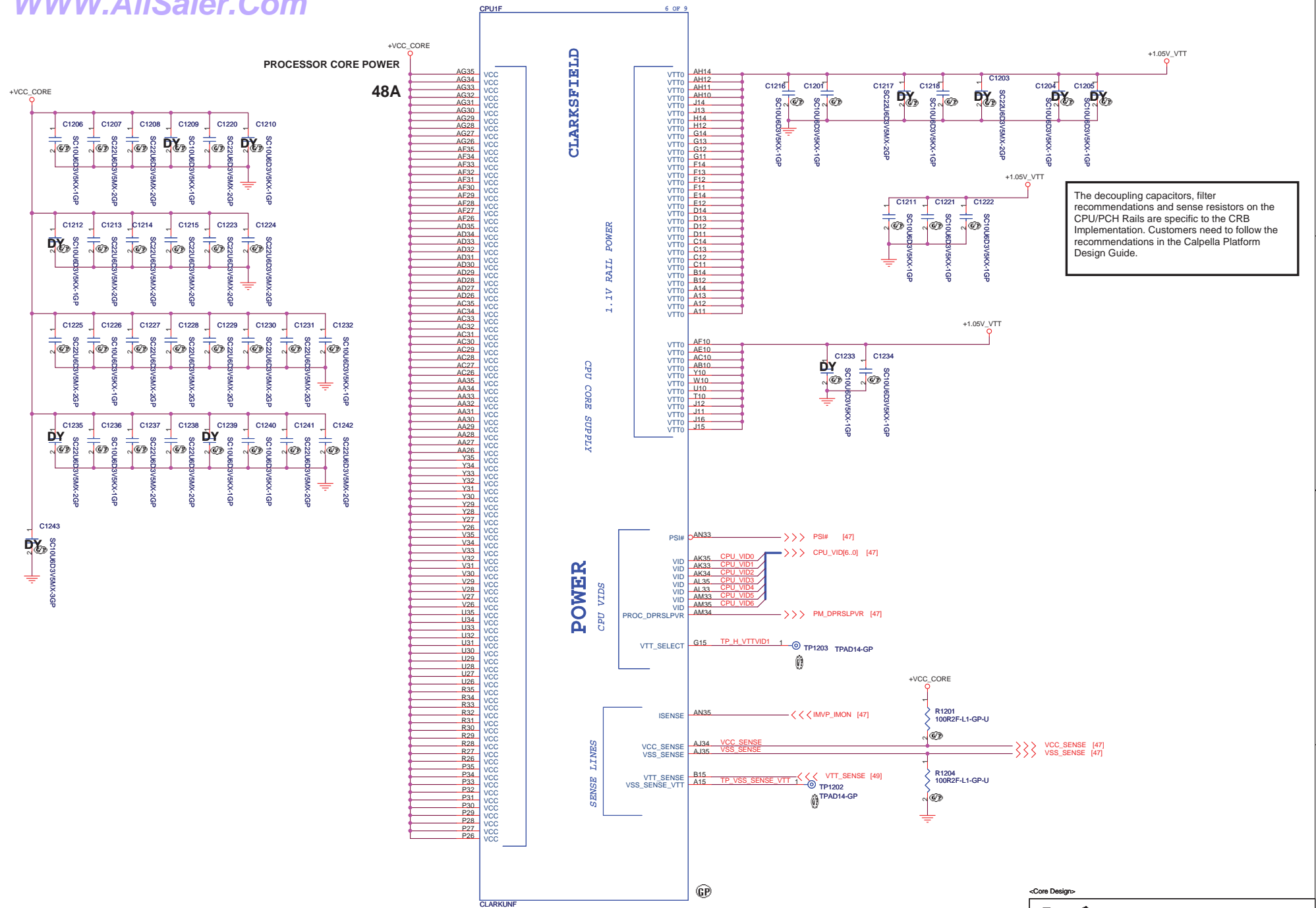
DELL		Wistron Corporation	
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Title			
CPU (PCIe/DMI/FDI)			
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CPU (THERMAL/CLOCK/PM)			
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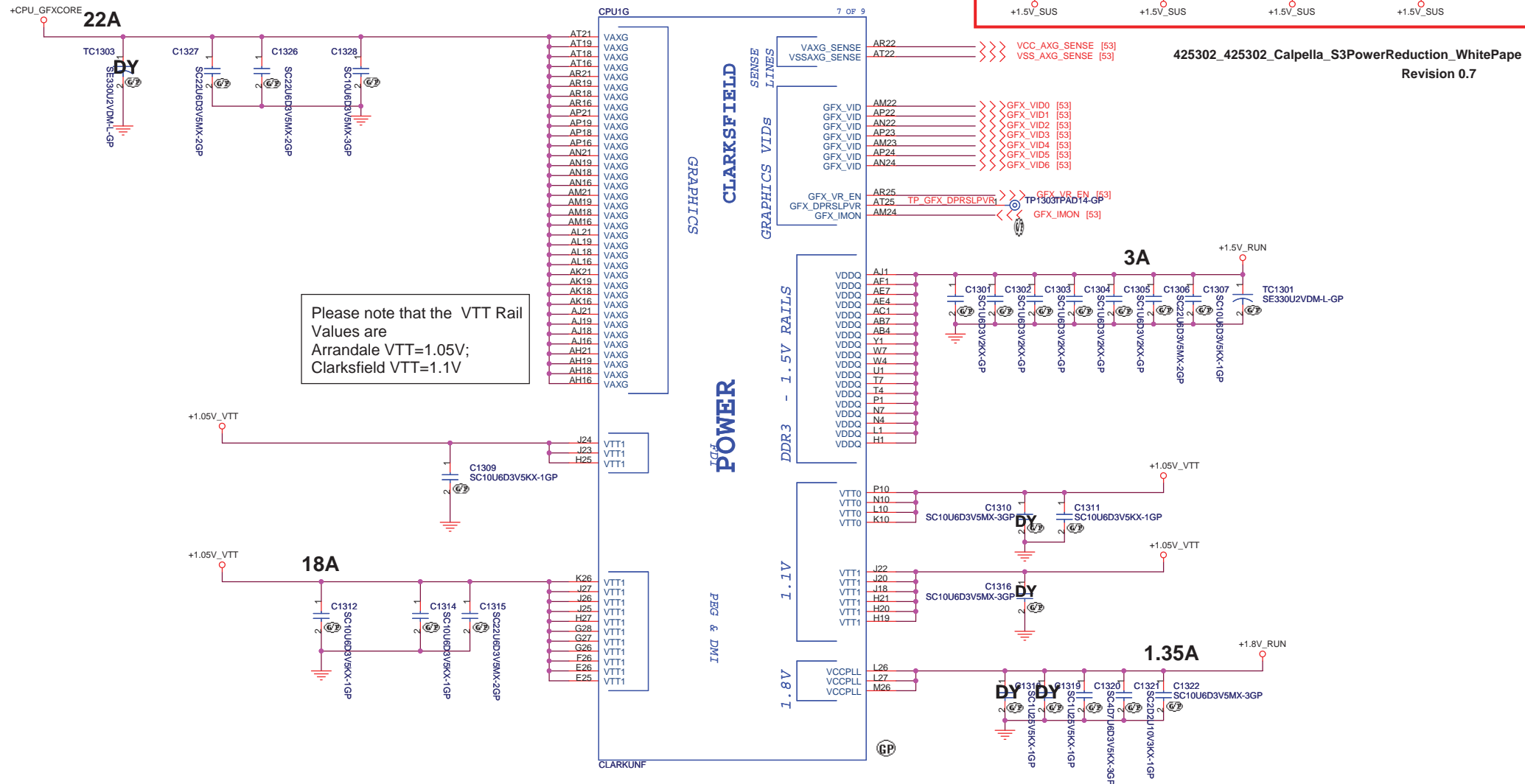


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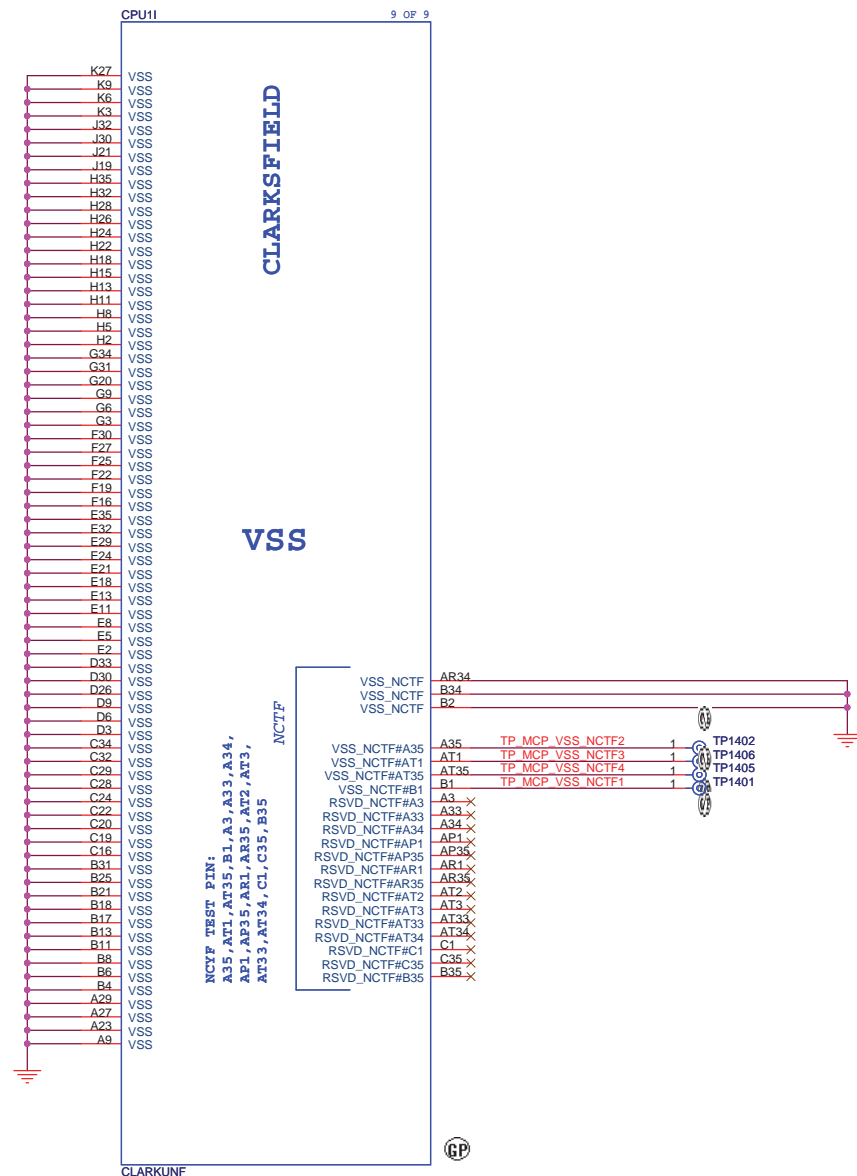
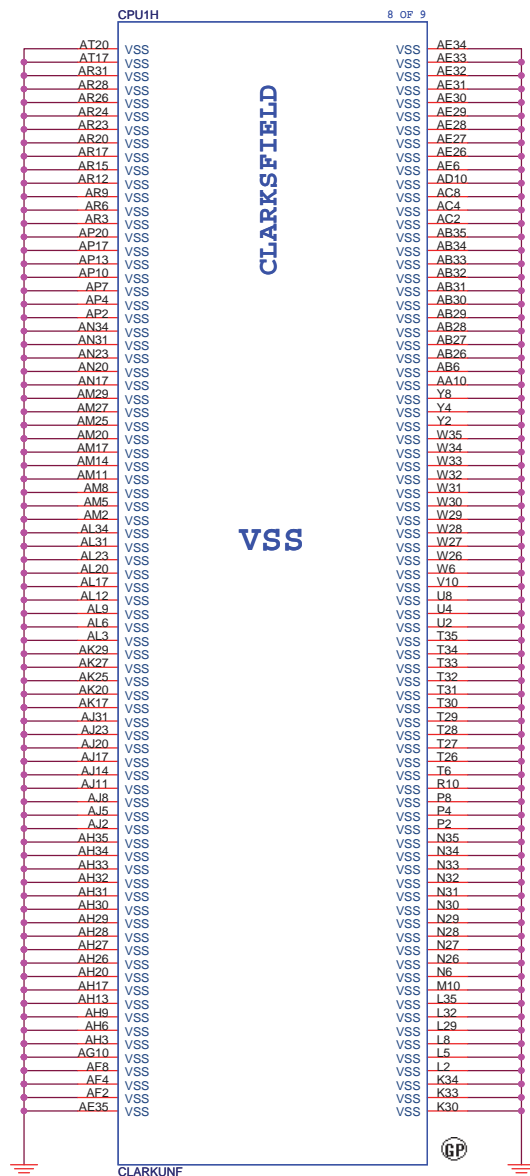


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Title				
CPU (VSS)				
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Title


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<Core Design>



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Title

(Reserve)

Size
Custom

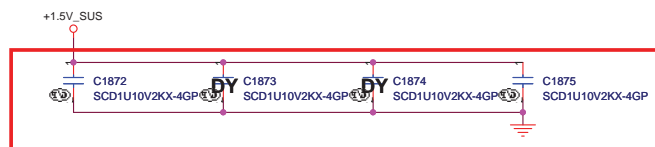
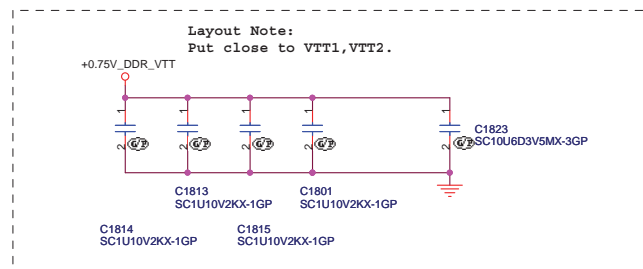
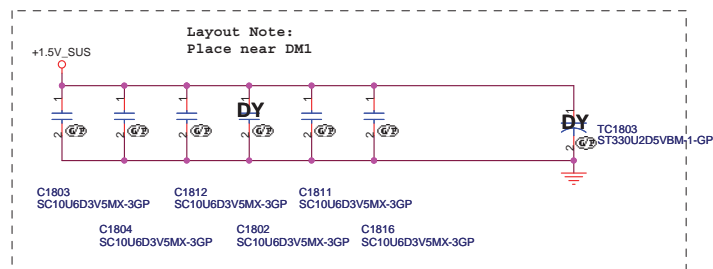
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Vostro Calpella

Rev
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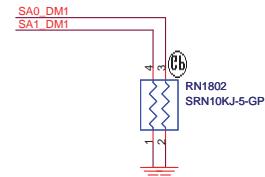
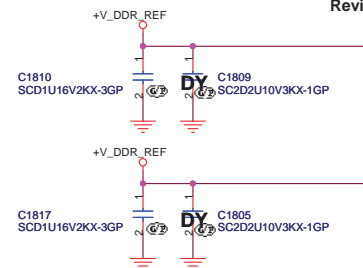
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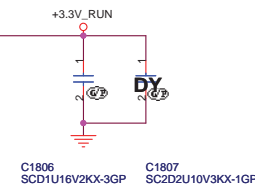
```
[10] M_A_DQS#[7..0] << >>
[10] M_A_DQ[63..0] << >>
[10] M_A_DM[7..0] << >>
[10] M_A_DQS[7..0] << >>
[10] M_A_A[15..0] << >>
```



425302_425302_Calpella_S3PowerReduction_WhitePaper
Revision 0.7



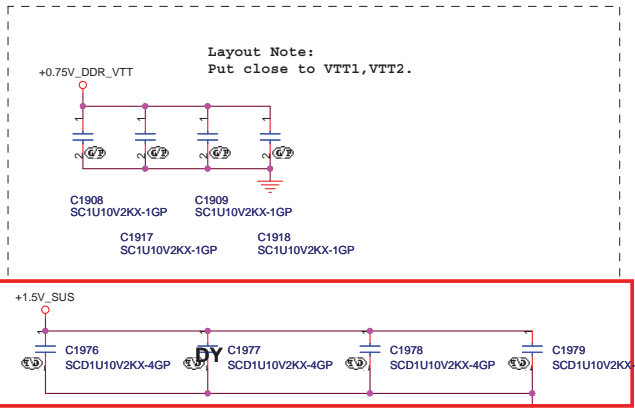
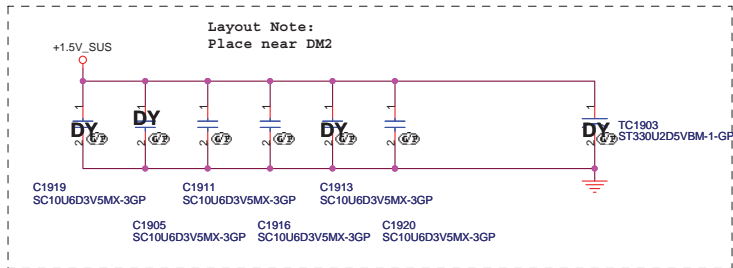
SMBUS address:A0



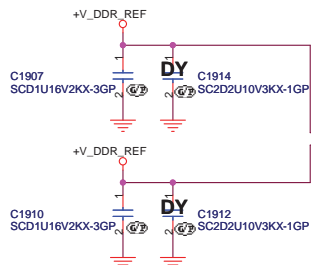
Height 5.2mm

62.10017.P31

[10] M_B_DQS# [7..0] << >>
[10] M_B_DQ [63..0] << >>
[10] M_B_DM [7..0] << >>
[10] M_B_DQS [7..0] << >>
[10] M_B_A [15..0] << >>

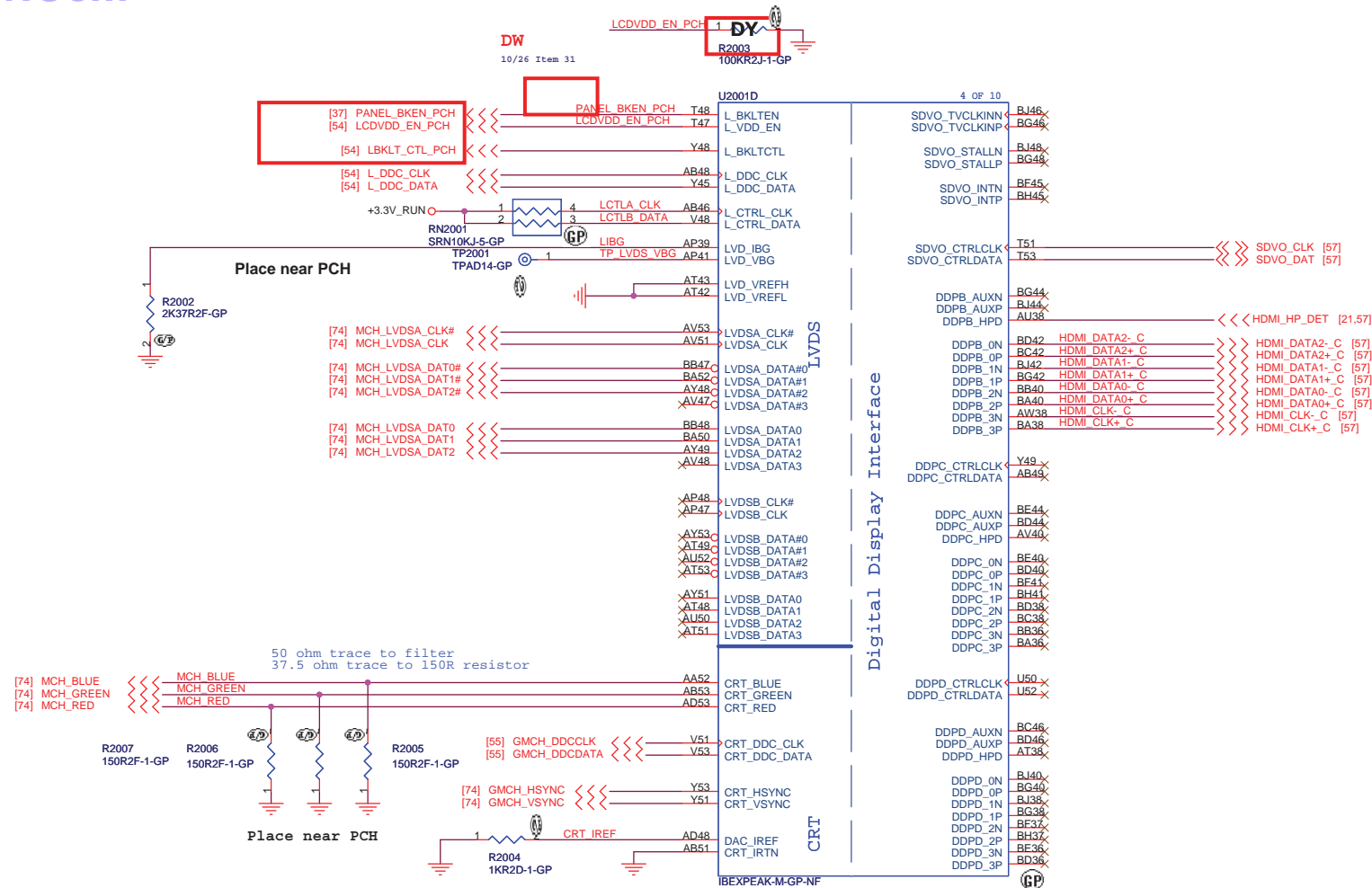


425302_425302_Calpella_S3PowerReduction_WhitePage
Revision 0.7



[10] M_ODT2 >>> M_ODT2
[10] M_ODT3 >>> M_ODT3
[9,18] DDR3_DRAMRST# >>>
+0.75V_DDR_VTT
VTT1
VTT2

M_B A0	98	A0	NP1	NP1
M_B A1	97	A1	NP2	NP2
M_B A2	96	A2	RAS#	110
M_B A3	95	A3	WE#	113
M_B A4	92	A4	CAS#	115
M_B A5	91	A5	CS0#	114
M_B A6	90	A6	CS1#	121
M_B A7	86	A7	CKE0	73
M_B A8	89	A8	CKE1	74
M_B A9	85	A9	A10/AP	101
M_B A10	107	A10	CK0	103
M_B A11	84	A11	CK0#	103
M_B A12	83	A12	CK1	102
M_B A13	119	A13	CK1#	104
M_B A14	80	A14	DM0	11
M_B A15	78	A15	DM1	28
M_B BS2	79	A16/BA2	DM2	46
M_B BS0	109	BA0	DM3	63
M_B BS1	108	BA1	DM4	136
M_B DQ0	5	DQ0	DM5	153
M_B DQ1	7	DQ1	DM6	170
M_B DQ2	15	DQ2	DM7	187
M_B DQ3	17	DQ3	SDA	200
M_B DQ4	4	DQ4	SCL	202
M_B DQ5	6	DQ5	EVENT#	198
M_B DQ6	16	DQ6	VDDSPD	199
M_B DQ7	18	DQ7	SA0	197
M_B DQ8	21	DQ8	SA1	201
M_B DQ9	23	DQ9	NC#1	77
M_B DQ10	33	DQ10	NC#2	122
M_B DQ11	35	DQ11	NC#2	125
M_B DQ12	22	DQ12	NC#2	125
M_B DQ13	24	DQ13	VDD1	75
M_B DQ14	34	DQ14	VDD2	76
M_B DQ15	36	DQ15	VDD3	81
M_B DQ16	39	DQ16	VDD4	82
M_B DQ17	41	DQ17	VDD5	87
M_B DQ18	51	DQ18	VDD6	88
M_B DQ19	53	DQ19	VDD7	93
M_B DQ20	40	DQ20	VDD8	94
M_B DQ21	42	DQ21	VDD9	99
M_B DQ22	50	DQ22	VDD10	100
M_B DQ23	52	DQ23	VDD11	105
M_B DQ24	57	DQ24	VDD12	106
M_B DQ25	59	DQ25	VDD13	111
M_B DQ26	67	DQ26	VDD14	112
M_B DQ27	69	DQ27	VDD15	117
M_B DQ28	56	DQ28	VDD16	118
M_B DQ29	58	DQ29	VDD17	123
M_B DQ30	68	DQ30	VDD18	124
M_B DQ31	70	DQ31	VSS	2
M_B DQ32	129	DQ32	VSS	3
M_B DQ33	131	DQ33	VSS	8
M_B DQ34	141	DQ34	VSS	9
M_B DQ35	143	DQ35	VSS	13
M_B DQ36	130	DQ36	VSS	14
M_B DQ37	132	DQ37	VSS	19
M_B DQ38	140	DQ38	VSS	20
M_B DQ39	142	DQ39	VSS	25
M_B DQ40	147	DQ40	VSS	31
M_B DQ41	149	DQ41	VSS	32
M_B DQ42	157	DQ42	VSS	37
M_B DQ43	159	DQ43	VSS	38
M_B DQ44	146	DQ44	VSS	43
M_B DQ45	148	DQ45	VSS	44
M_B DQ46	158	DQ46	VSS	48
M_B DQ47	160	DQ47	VSS	49
M_B DQ48	163	DQ48	VSS	54
M_B DQ49	165	DQ49	VSS	55
M_B DQ50	175	DQ50	VSS	60
M_B DQ51	177	DQ51	VSS	61
M_B DQ52	164	DQ52	VSS	65
M_B DQ53	166	DQ53	VSS	66
M_B DQ54	174	DQ54	VSS	71
M_B DQ55	176	DQ55	VSS	72
M_B DQ56	181	DQ56	VSS	127
M_B DQ57	183	DQ57	VSS	128
M_B DQ58	191	DQ58	VSS	133
M_B DQ59	193	DQ59	VSS	134
M_B DQ60	180	DQ60	VSS	138
M_B DQ61	182	DQ61	VSS	139
M_B DQ62	192	DQ62	VSS	144
M_B DQ63	194	DQ63	VSS	145
M_B DQS#0	10	DQS0	VSS	150
M_B DQS#1	22	DQS1	VSS	151
M_B DQS#2	45	DQS2	VSS	155
M_B DQS#3	62	DQS3	VSS	156
M_B DQS#4	135	DQS4	VSS	161
M_B DQS#5	152	DQS5	VSS	162
M_B DQS#6	168	DQS6	VSS	167
M_B DQS#7	186	DQS7	VSS	168
M_B DQSO	12	DQSO	VSS	172
M_B DQS1	29	DQS1	VSS	173
M_B DQS2	47	DQS2	VSS	178
M_B DQS3	64	DQS3	VSS	179
M_B DQS4	137	DQS4	VSS	184
M_B DQS5	154	DQS5	VSS	185
M_B DQS6	171	DQS6	VSS	189
M_B DQS7	188	DQS7	VSS	190
M_B DQSO	12	DQSO	VSS	195
M_B DQS1	29	DQS1	VSS	196
M_B DQS2	47	DQS2	VSS	205
M_B DQS3	64	DQS3	VSS	206
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
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M_B DQS2	47	DQS2	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS2	47	DQS2	VSS	
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M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS2	47	DQS2	VSS	
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M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
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M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
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M_B DQS4	137	DQS4	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS3	64	DQS3	VSS	
M_B DQS4	137	DQS4	VSS	
M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1	29	DQS1	VSS	
M_B DQS2	47	DQS2	VSS	
M_B DQS3	64	DQS3	VSS	
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M_B DQS5	154	DQS5	VSS	
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M_B DQS7	188	DQS7	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
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M_B DQS5	154	DQS5	VSS	
M_B DQS6	171	DQS6	VSS	
M_B DQS7	188	DQS7	VSS	
M_B DQSO	12	DQSO	VSS	
M_B DQS1				



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Title

PCH (LVDS/CRT/DDI)

Size

Document Number

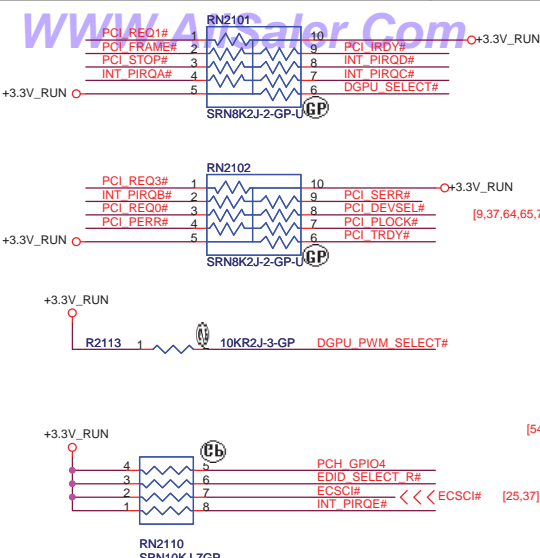
Rev

Vostro Calpella

X01

Date: Monday, January 18, 2010

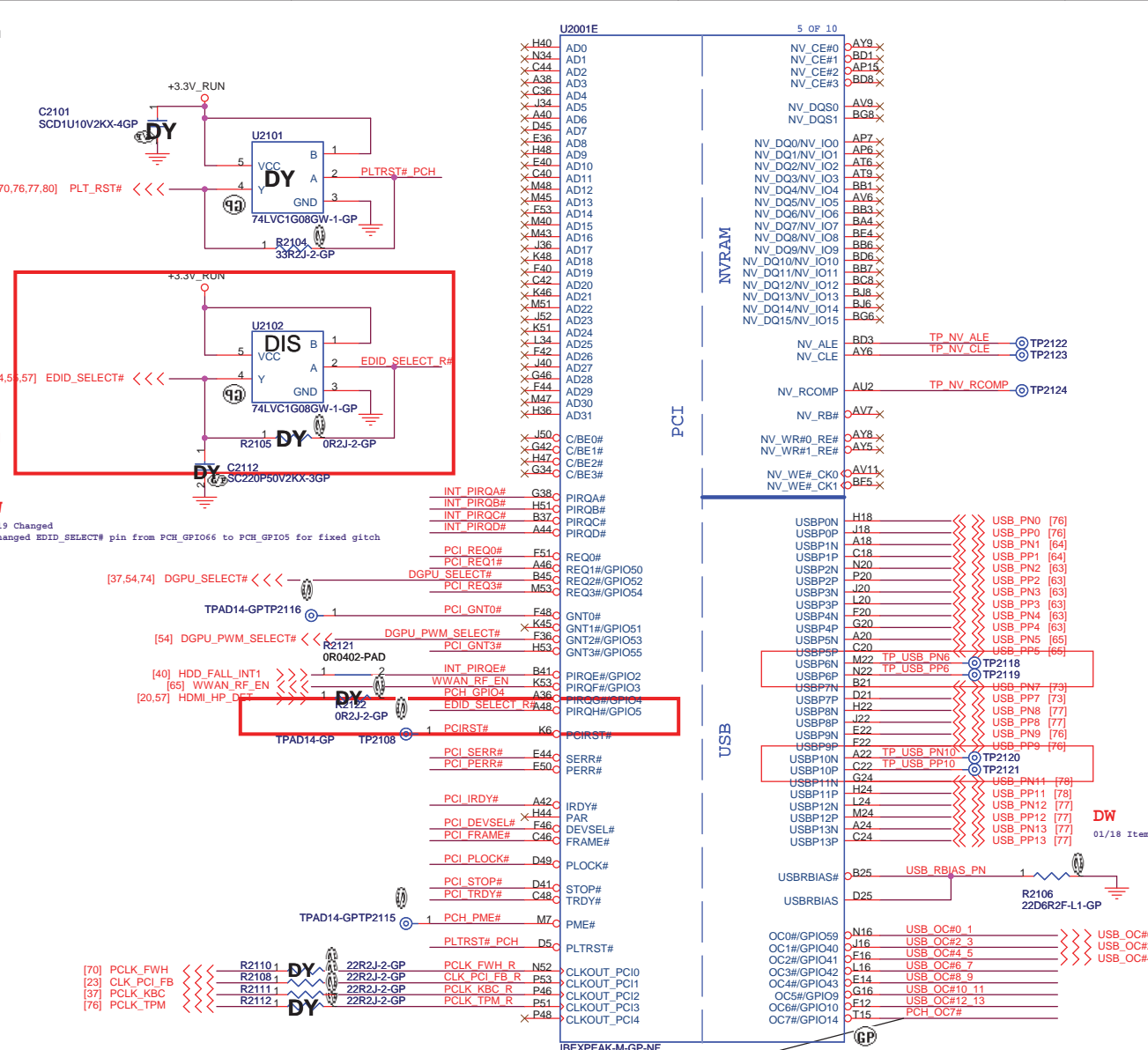
Sheet 20 of 91



DW 

10/19 Changed
1.Changed EDID_SELECT# pin from PCH_GPIO66 to PCH_GPIO5 for fixed gitch

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)



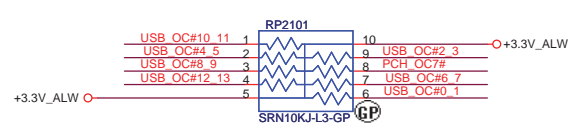
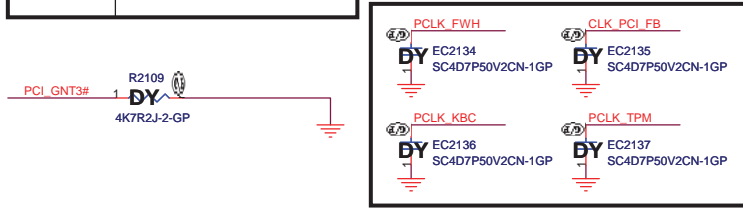
USB	
Pair	Device
0	USB1
1	WLAN
2	USB2
3	USB3
4	USB for ESATA
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	CAMERA
11	Biometric
12	New Card
13	CardReader

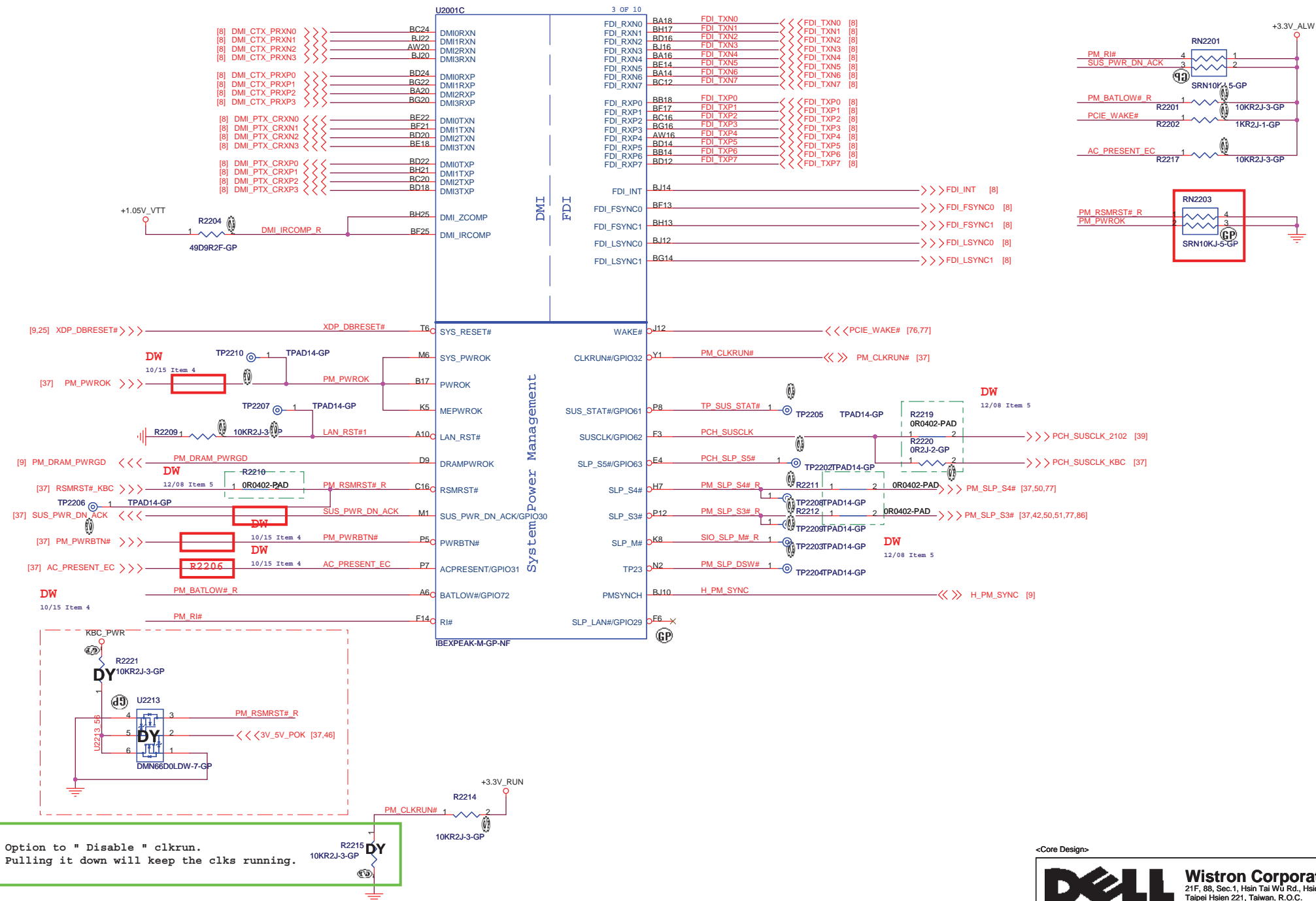
Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default

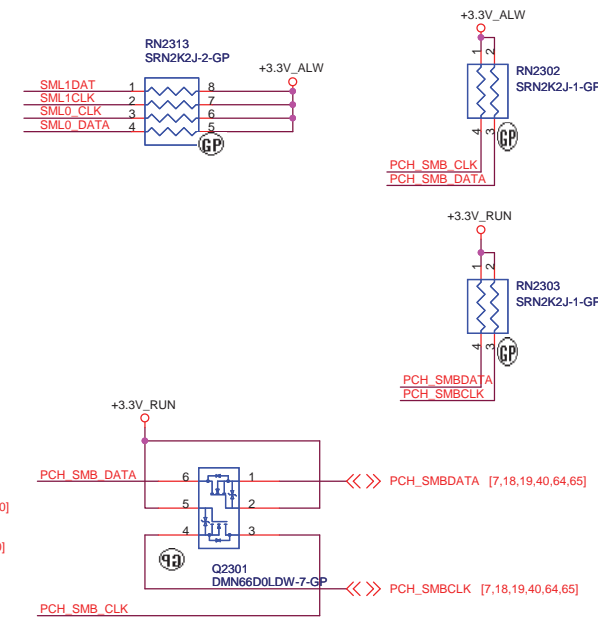
Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.







	C2313	C2307	X2301	R2380
Normal	0R2J-2-GP	DY	DY	DY
dale DCI	SC18P	SC18P	25MHZ	1MR

Figure 6

XTAL25 IN

XTAL25 OUT

R2380
1MR2J1-GP

X2301
XTAL-25MHZ-67GP

C2313
SC12P50V2JN-3GP

C2307
SC15P50V2JN-2GP

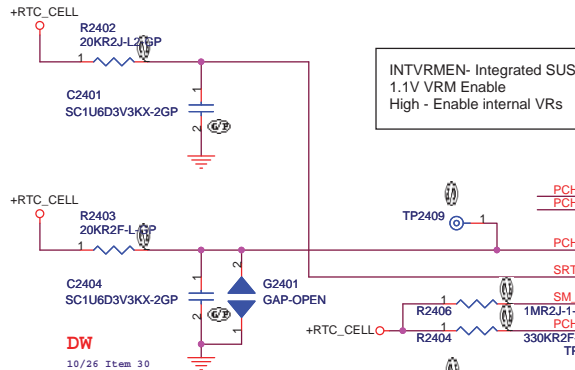
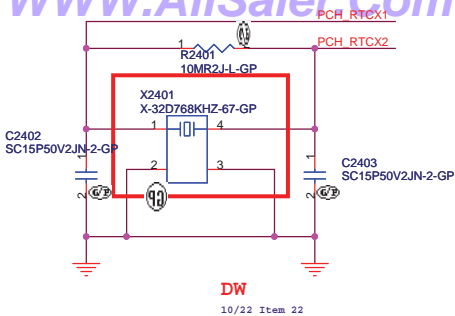
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Title	PCH (PCI-E/SMBUS/CLOCK/CL)
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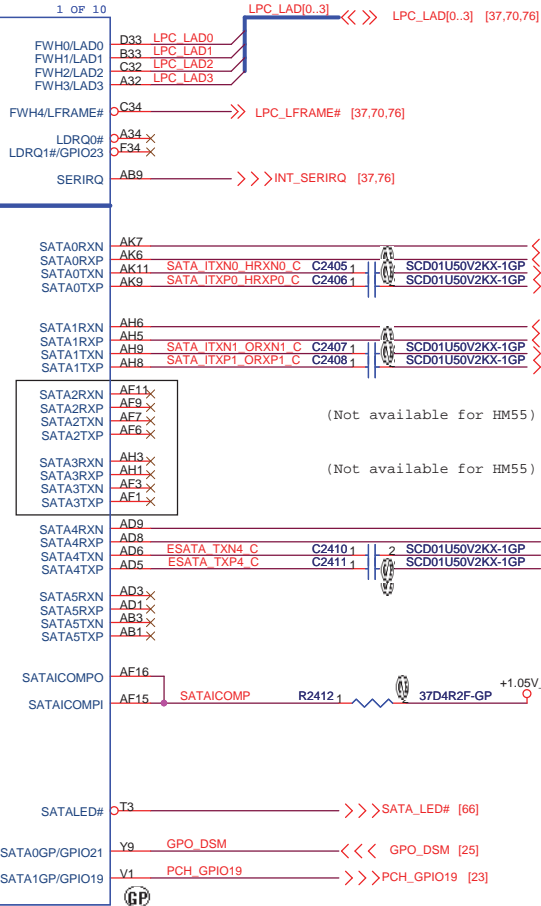
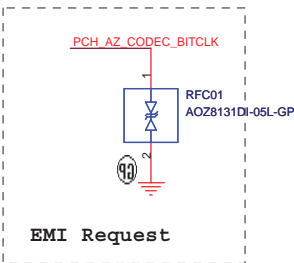
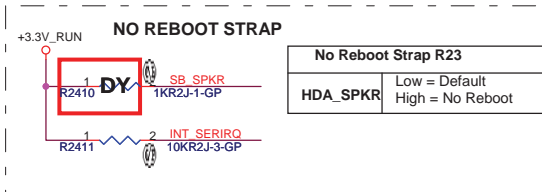
Size	Document Number	Rev
	Vostro Calpella	X
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Flash Descriptor Security Override/ ME Debug Mode

ME_UNLOCK#

This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.



HDD

ODD

ESATA

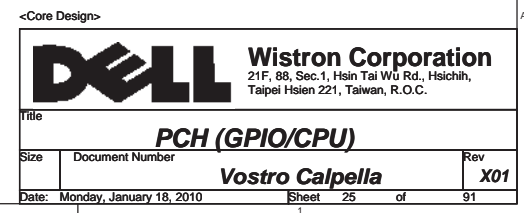
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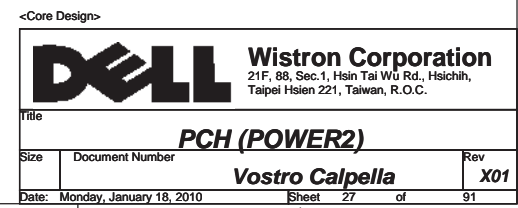
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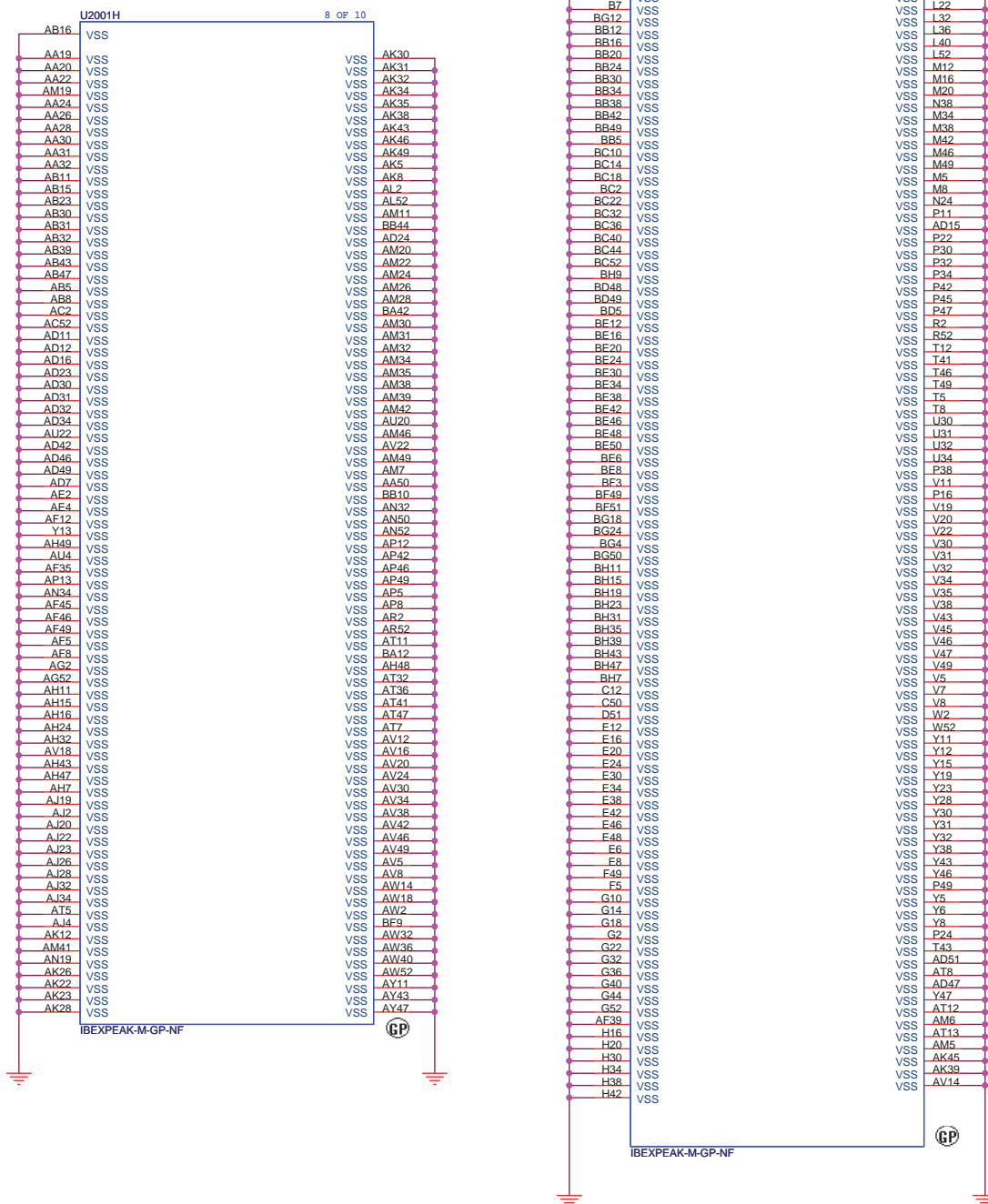
Size: Document Number Rev: **X01**

Date: Monday, January 18, 2010 Sheet 24 of 91









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Title

PCH (VSS)

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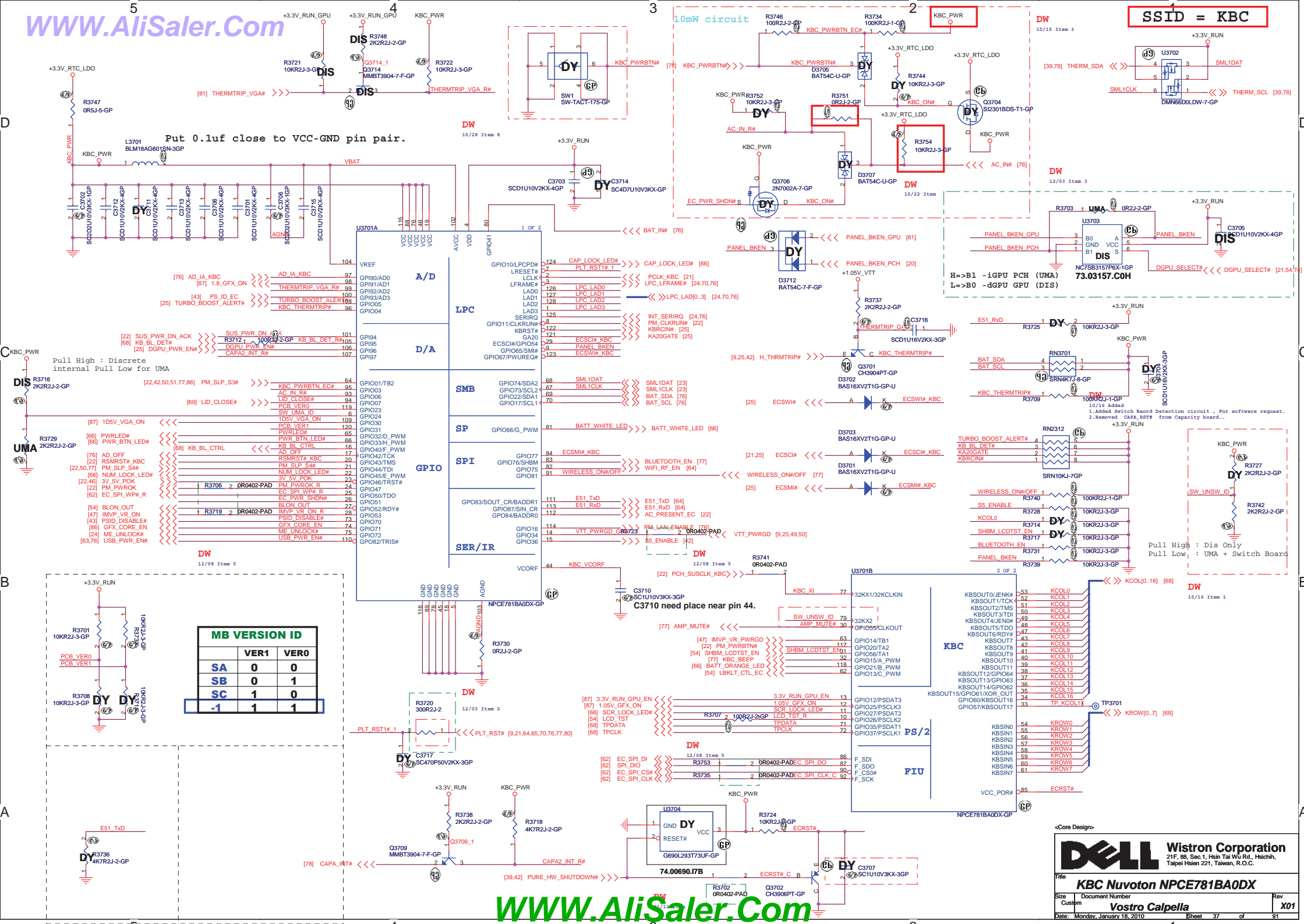
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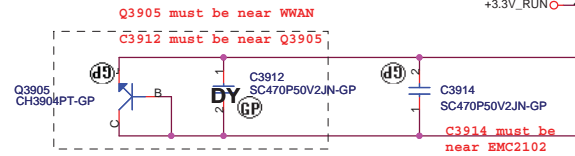
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Document Number
Vostro Calpella

Rev
X01

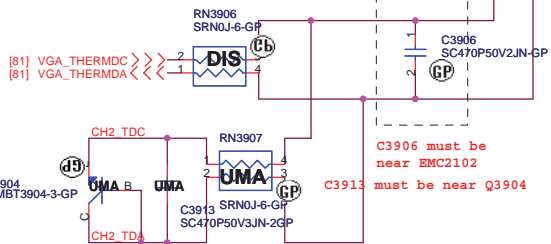
Date: Monday, January 18, 2010Sheet 38 of 91

1. WWAN



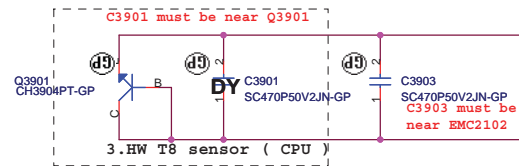
Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor



2. CPU Sensor

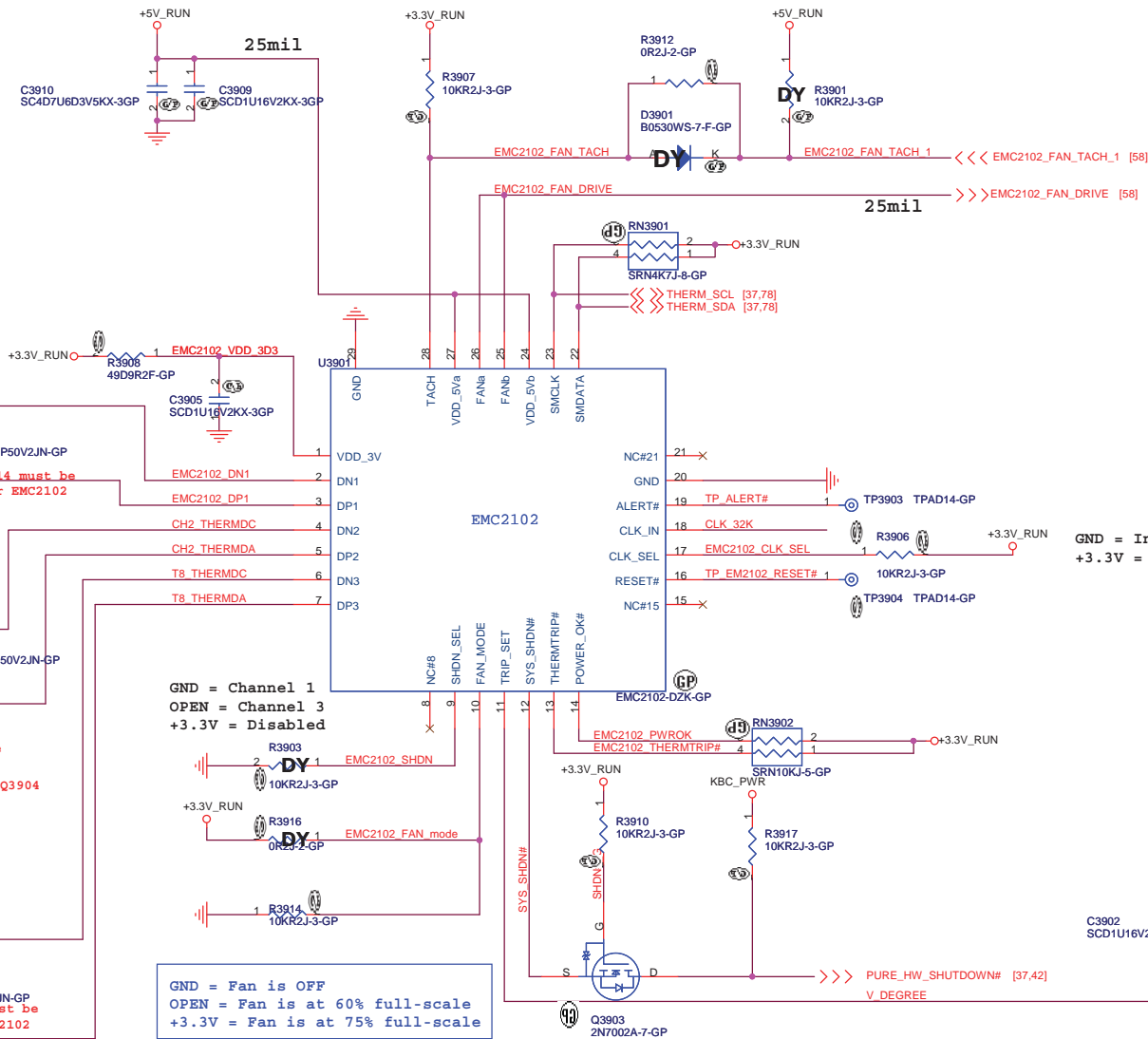
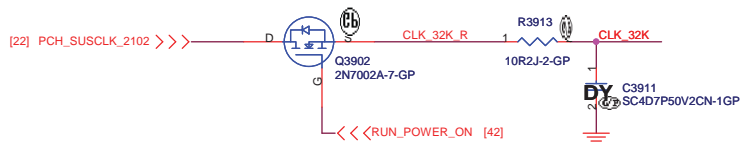
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.



3. HW T8 sensor (CPU)

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

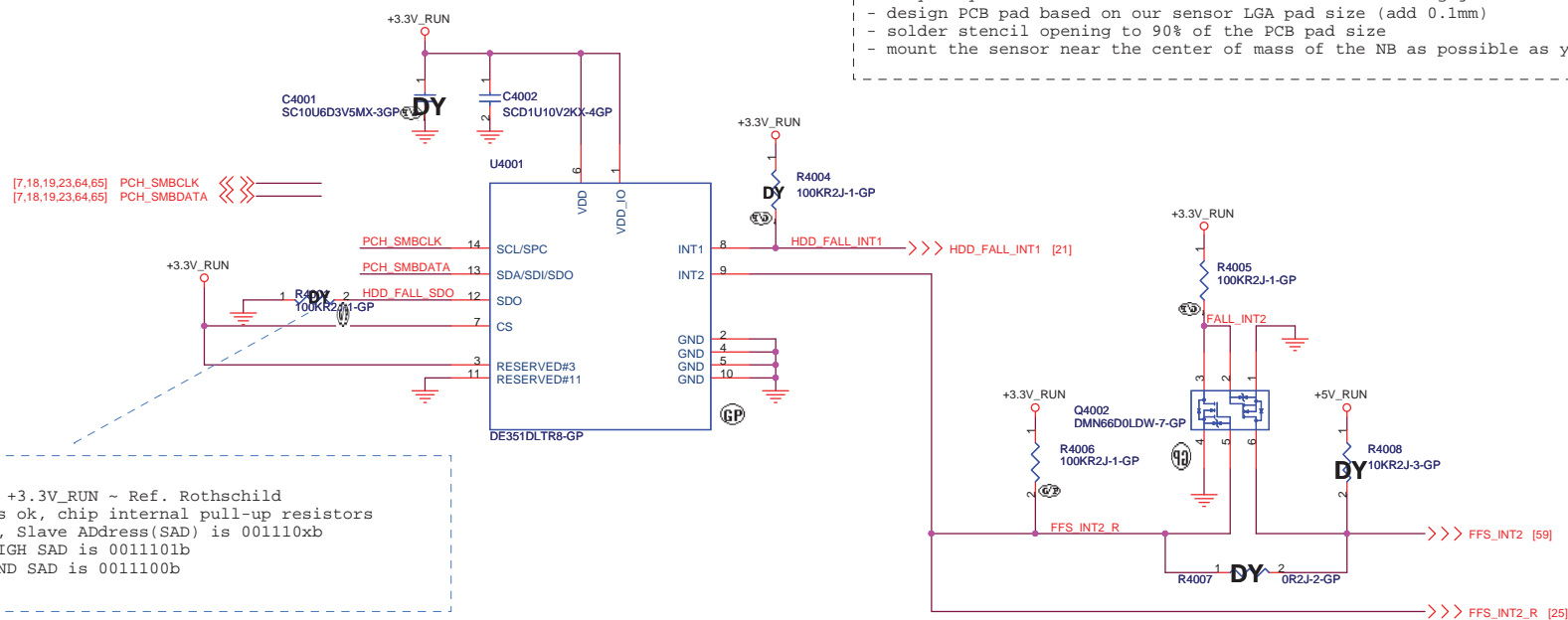
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

TRIP_SET Pin Voltage
 $V_DEGREE = (((Degree - 75) / 21))$
T8 shutdown is set 86 deg-C.

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Title: Thermal/Fan Controllor EMC2102			
Size: Custom	Document Number: Vostro Calpella	Rev: X01	
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Free Fall Sensor



```
09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave Address(SAD) is 001110xb
    Pull HIGH SAD is 0011101b
    Pull GND SAD is 0011100b
```

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

```
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can
```


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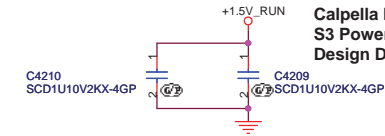
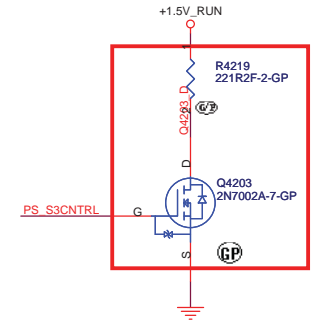
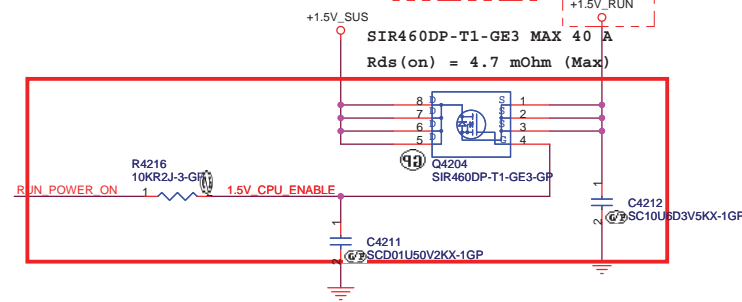
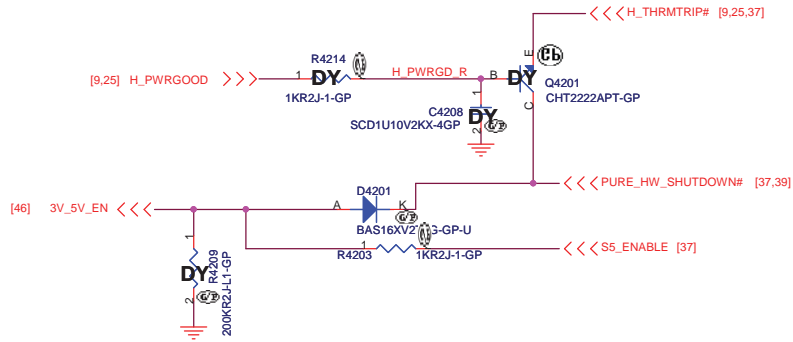
+1.5V_RUN:

Peak current: 4650 mA

Design current: 3255 mA

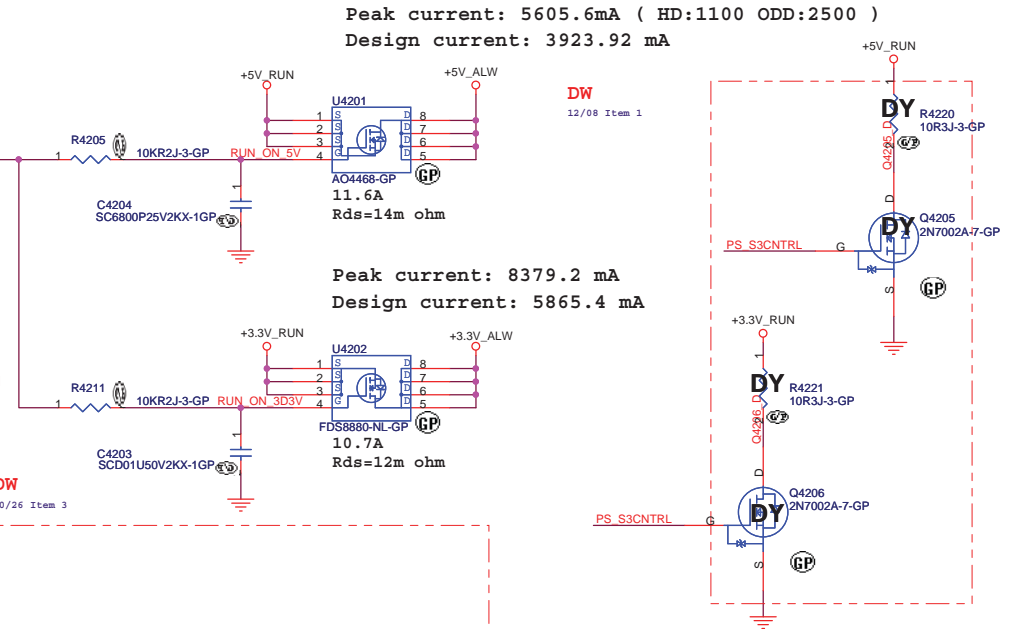
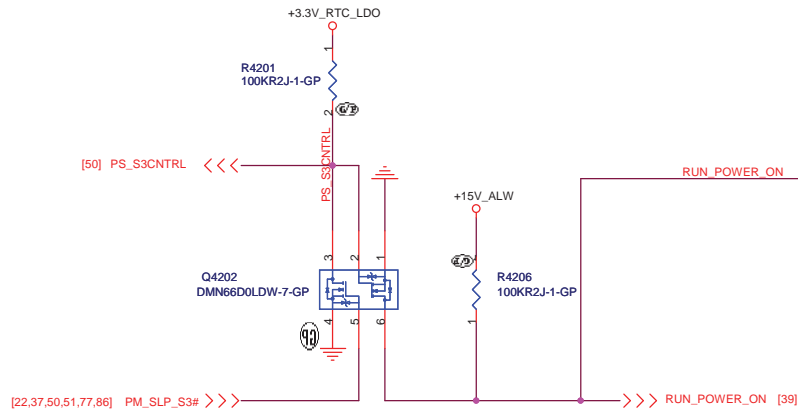
DW

10/26 Item 3



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

Revision 0.1



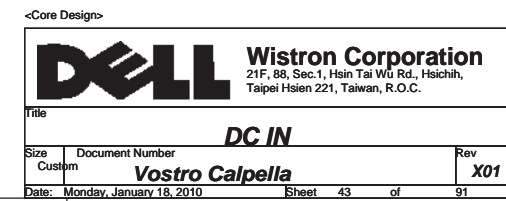
Peak current: 5605.6mA (HD:1100 ODD:2500)

Design current: 3923.92 mA

Peak current: 8379.2 mA


Design current: 5865.4 mA

<Core Design>



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<Core Design>



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Title


(Reserve)

Size	Document Number	Rev
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

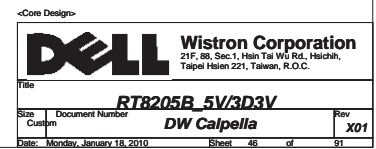
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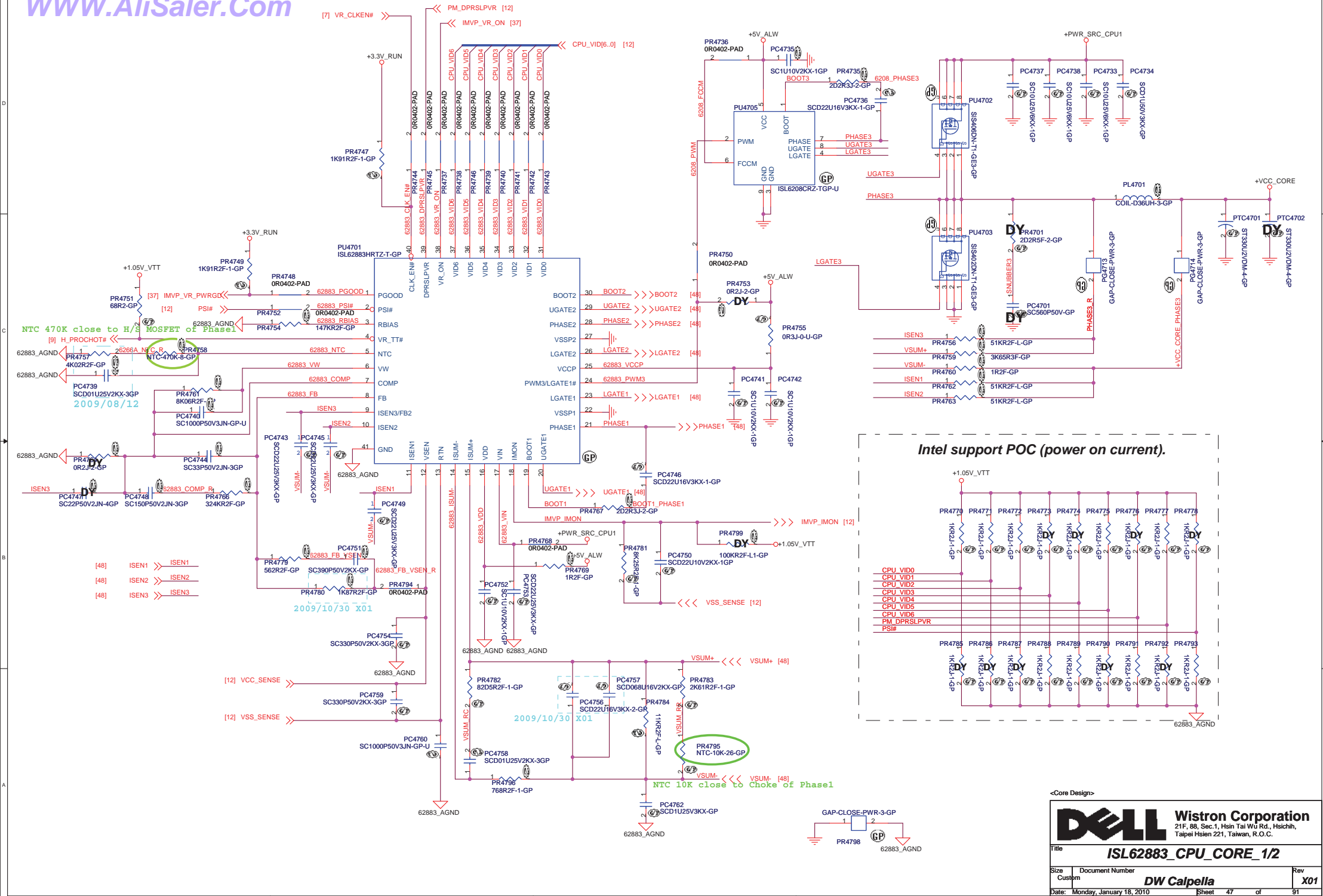
Size
Custom

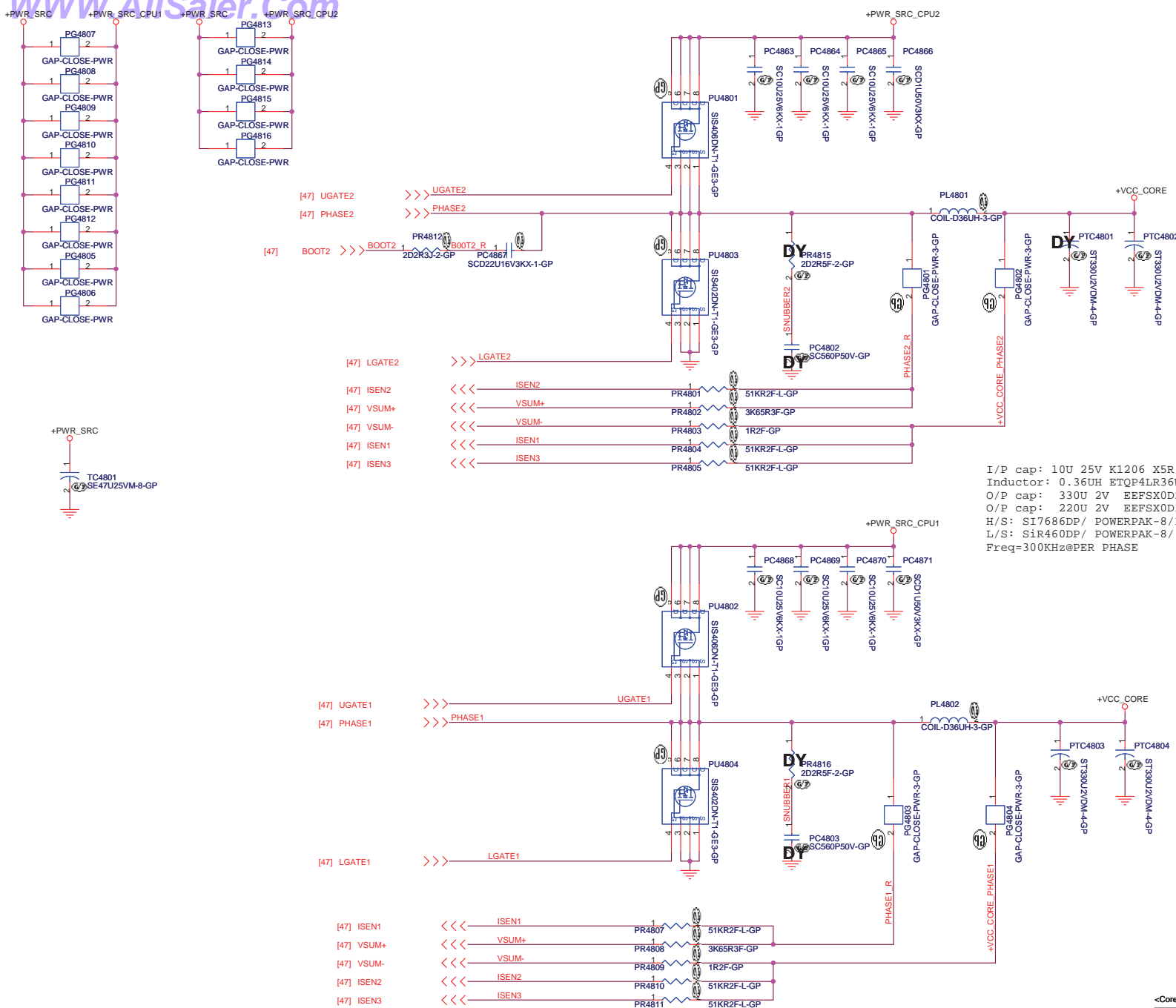
Document Number
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DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

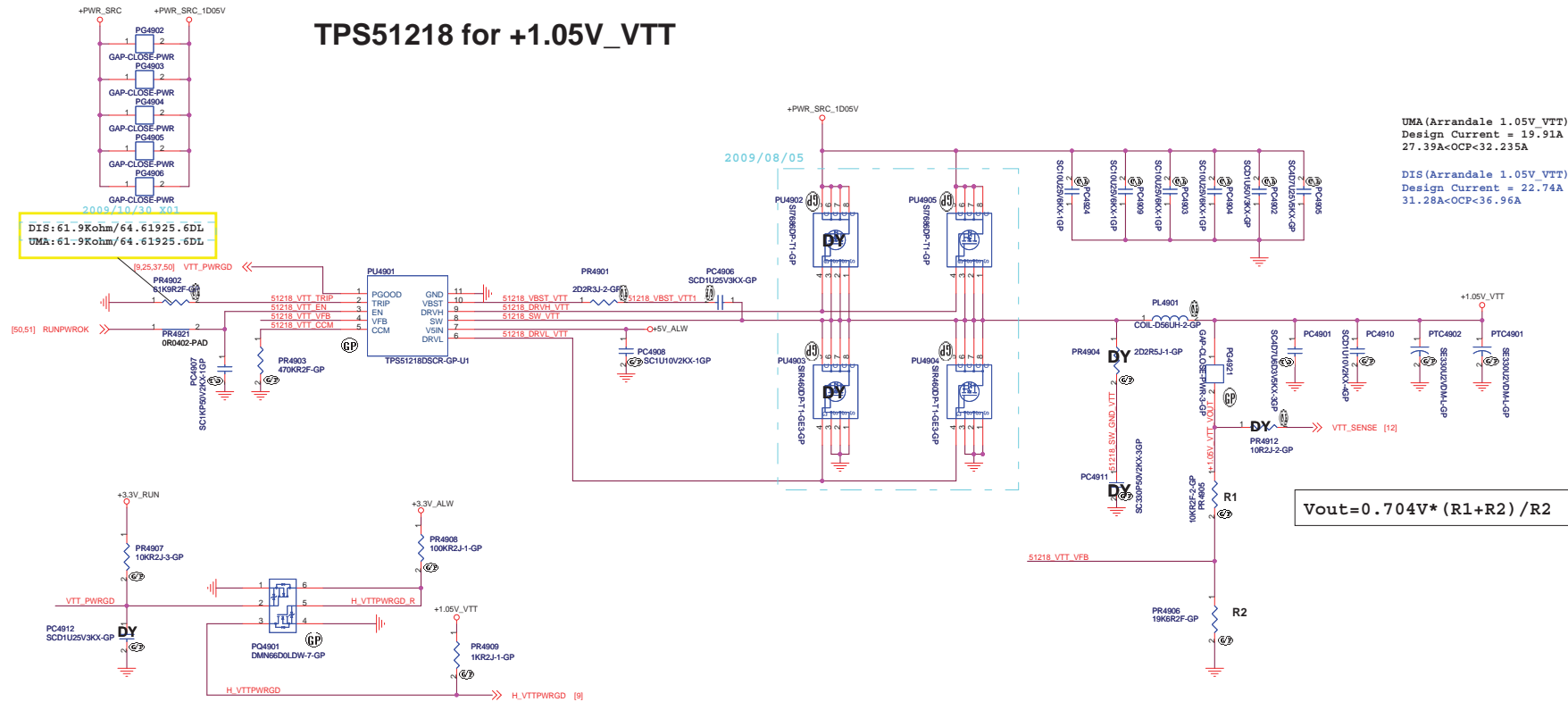
UMA(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Freq=300KHz@PER PHASE

<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ISL62883_CPU_CORE_2/2			
Size Custom	Document Number DW Calpella	Rev X01	
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TPS51218 for +1.05V_VTT



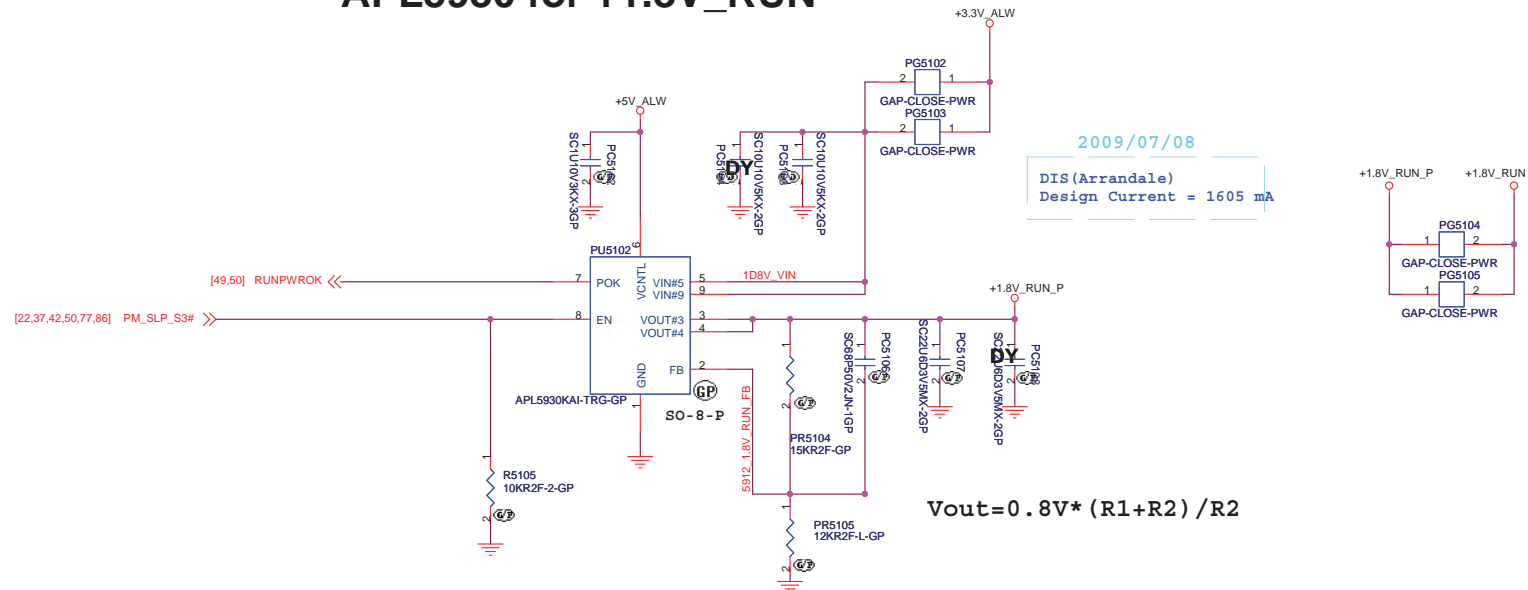
Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIR474DP-T1-GE3/10mohm/ 12mOhm@4.5Vgs/ 84.00474.037
L/S: SI7170DP-T1-GE3/3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037

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DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TPS51218 +1.05V VTT			
Size	Document Number		Rev
Custom	DW Calpella		X01
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APL5930 for +1.8V_RUN




<Core Design>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title APL5930 +1.8V RUN			
Size Custom	Document Number DW Calpella		Rev X01
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

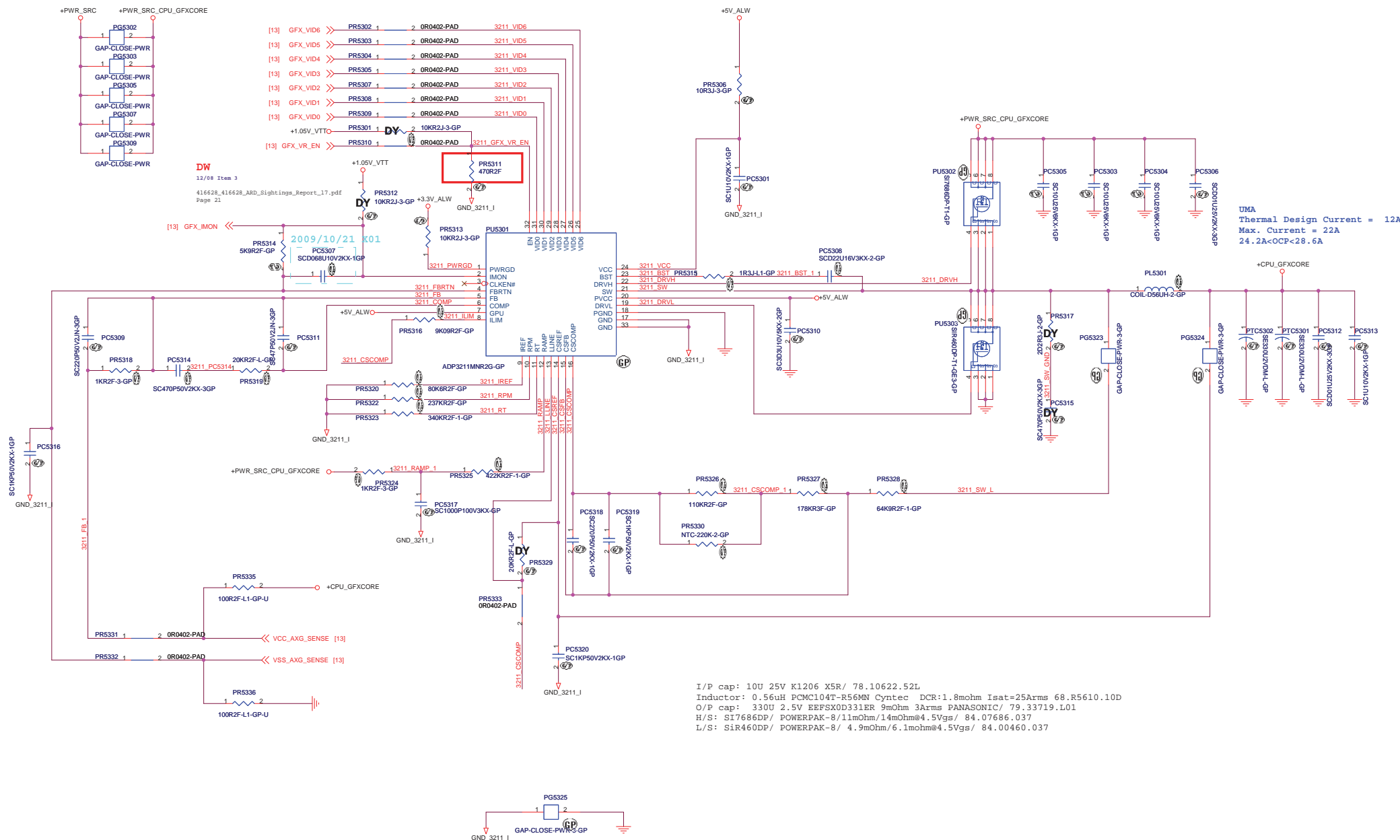
Size
Custom

Document Number
Vostro Calpella

Rev
X01

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```
SSID = CPU.GFX.Regulator
```



UMA
Thermal Design Current = 12A
Max. Current = 22A
24.2A<OCP<28.6A

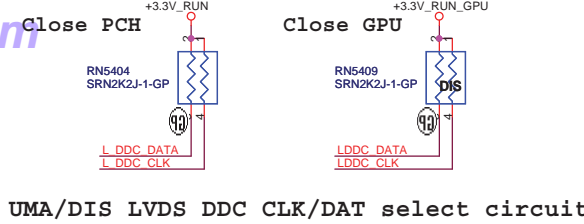
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56Mm Cyntec DCR=1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEF5033131ER 9n0hm 3ARms PANASONIC/ 79.33719.L01
H/S: ST1686DP/ POWERPAK-8/11m0hm/14m0hm@4.5Vgs/ 84.07686.037
L/S: S1R466DP/ POWERPAK-8/ 4.9m0hm/6.1mohm@4.5Vgs/ 84.04660.037



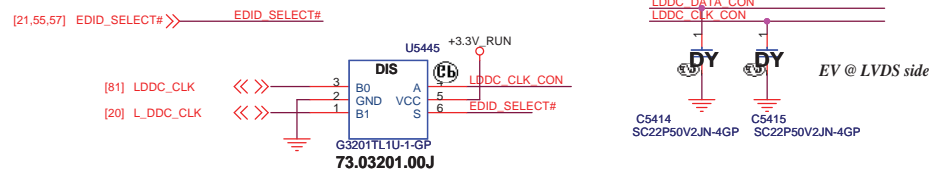
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
ADP3211 CPU GFXCORE			
Size	Document Number		Rev
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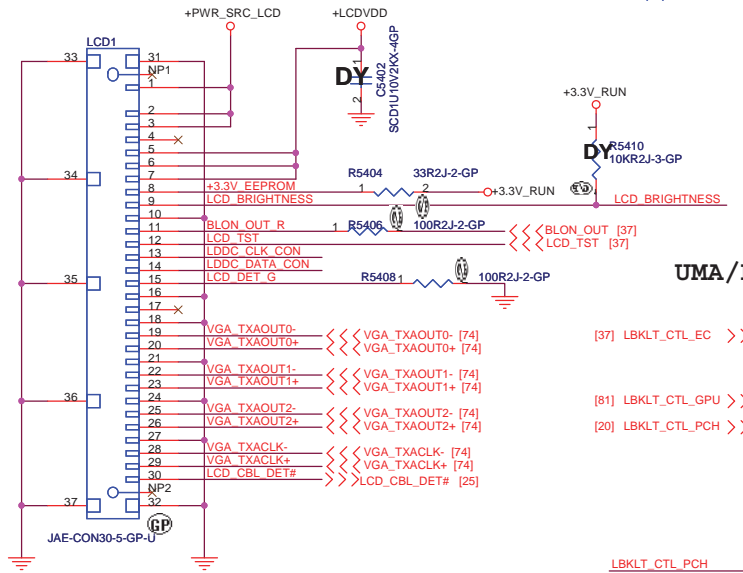
SSID = VIDEO



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

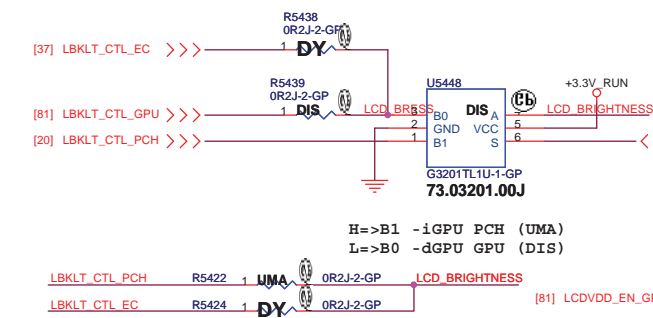


LVDS CONNECTOR

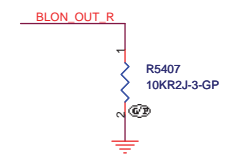
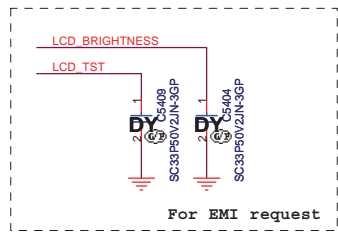


20.F1555.030

UMA/DIS LVDS PWM select circuit

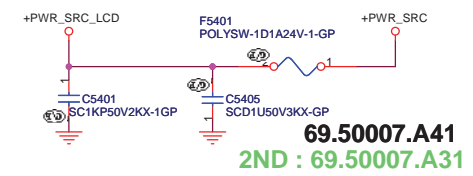


H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



SSID = Inverter

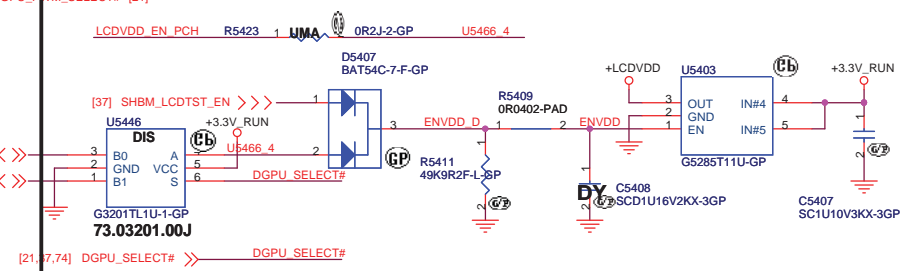
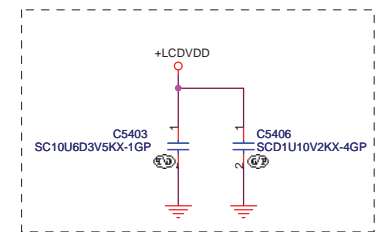
INVERTER POWER



69.50007.A41
2ND : 69.50007.A31

SSID = VIDEO

LCD POWER

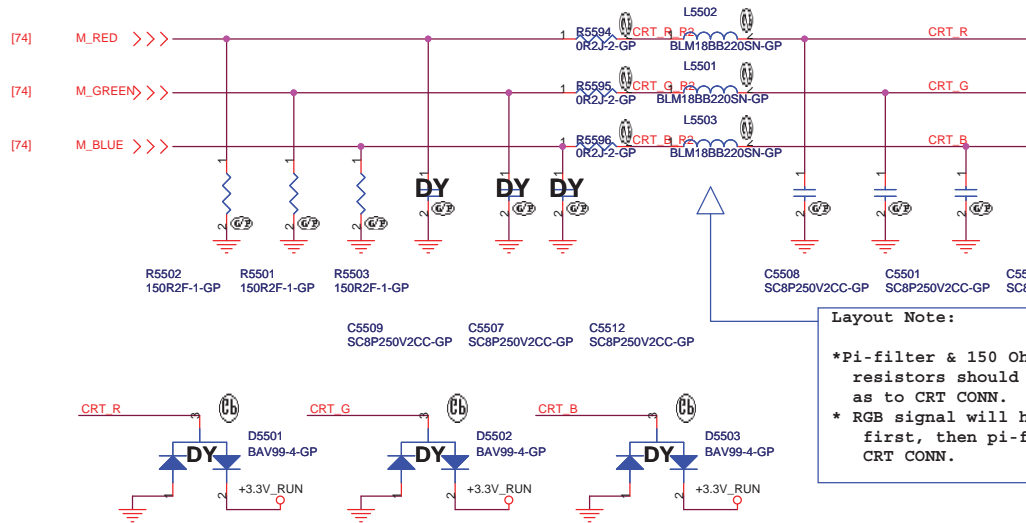


H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

<Core Design>

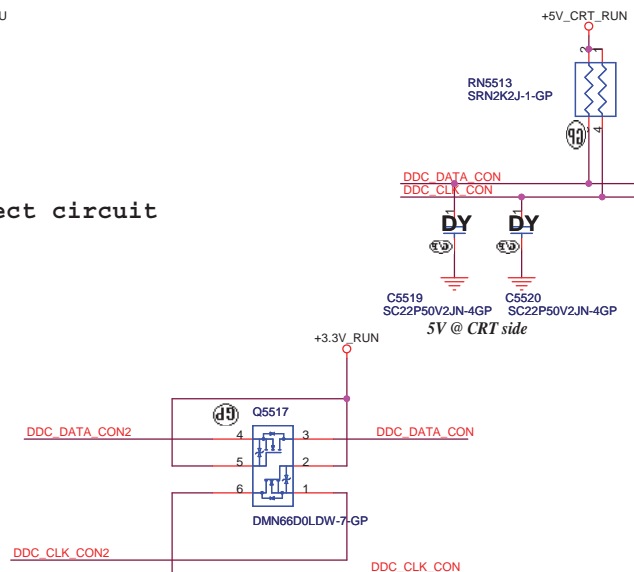
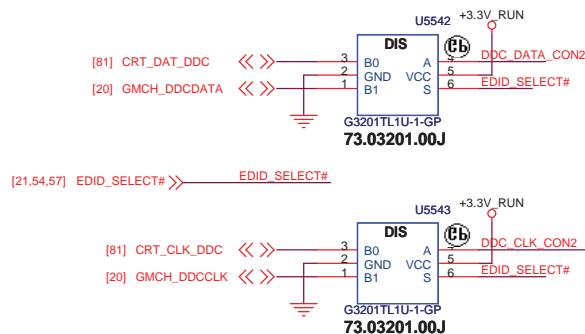
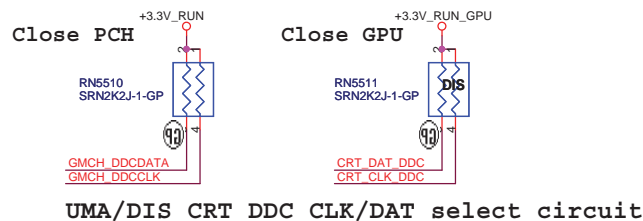
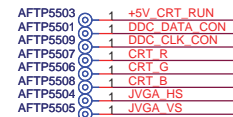
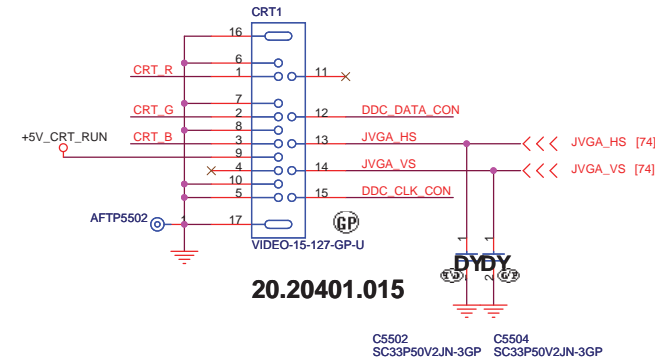
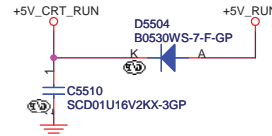
DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	LCD/Inverter Connector		
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SSID = VIDEO



Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.




H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



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<Core Design>



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Title

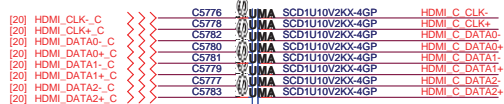
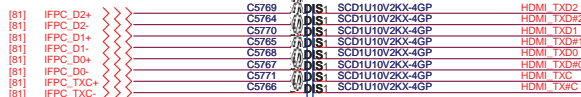
(Reserve)

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UMA/DIS HDMI signal select circuit

Place near connector

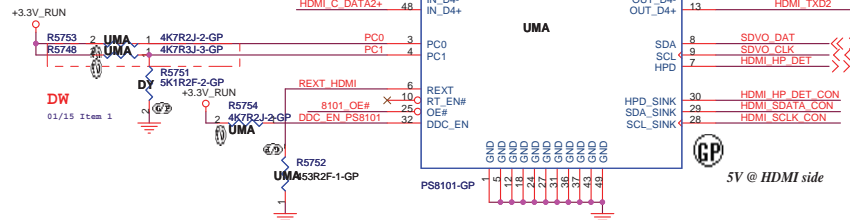


Close to PCH

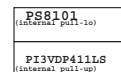
UMA HDMI level shift circuit

PS8101 TMD5 inputs equalization control

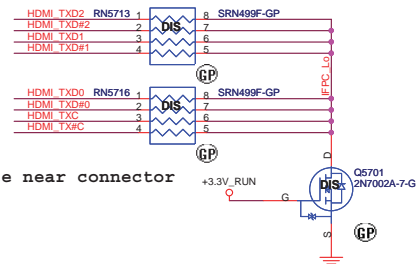
PC0	PC1	EQ
0	0	8db
0	1	4db
1	0	12db
1	1	0db



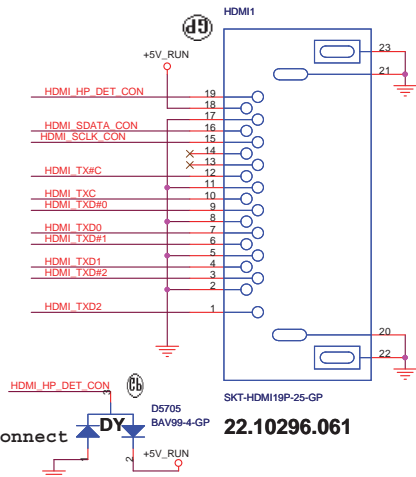
jitter elimination control



Place near connector

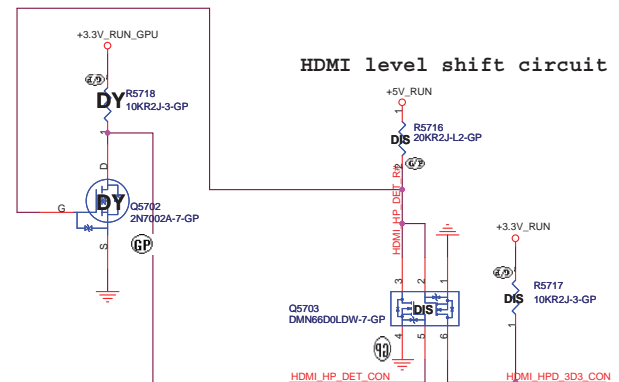


Close HDMI Connect

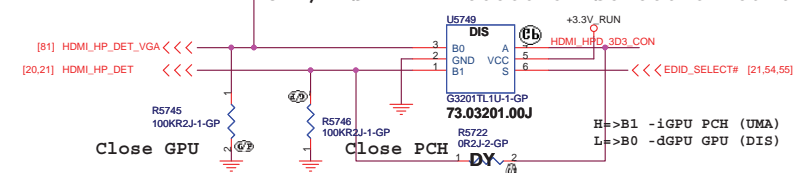


22.10296.061

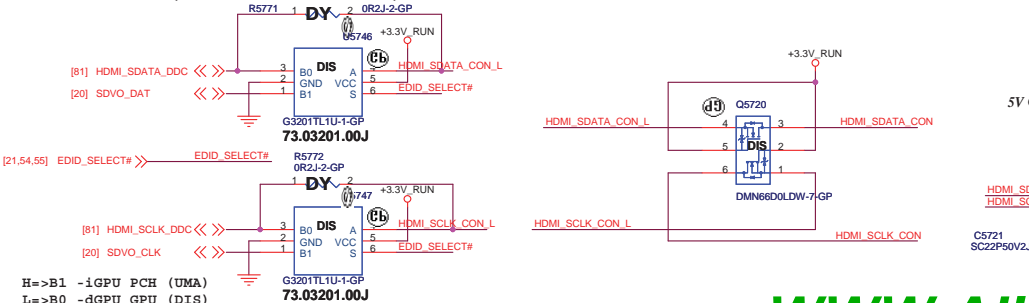
HDMI level shift circuit



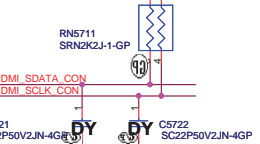
UMA/DIS HDMI Detection select circuit



UMA/DIS HDMI DDC CLK/DAT select circuit



5V @ HDMI side



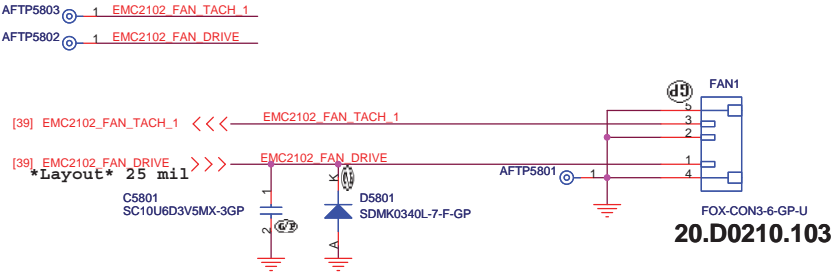
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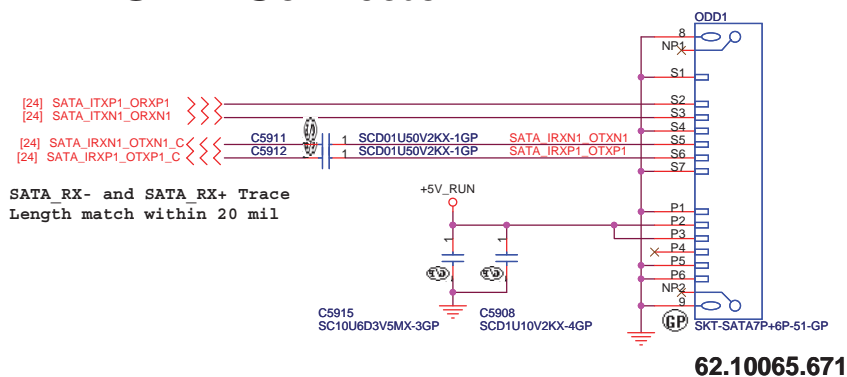
HDMI Connector		
Size	Document Number	Rev
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SSID = Thermal

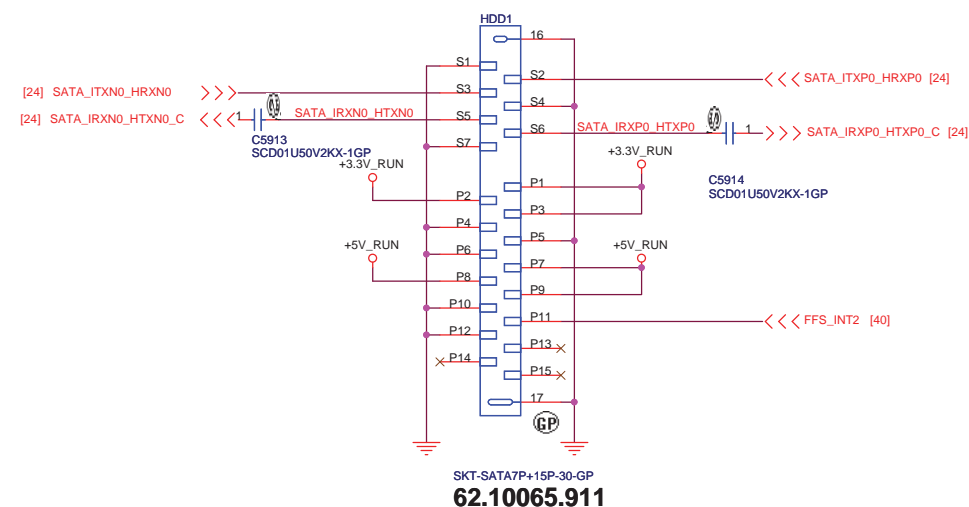
Fan Connector



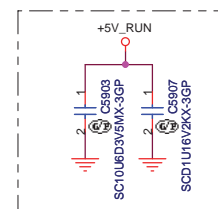
ODD Connector



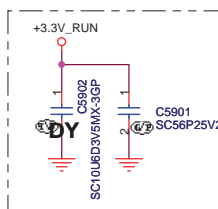
SATA HDD Connector



Close to CONN
5V power pin




Close to CONN
3.3V power pin



<Core Design>

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<Core Design>



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Title

(Reserve)

Size
Custom


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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

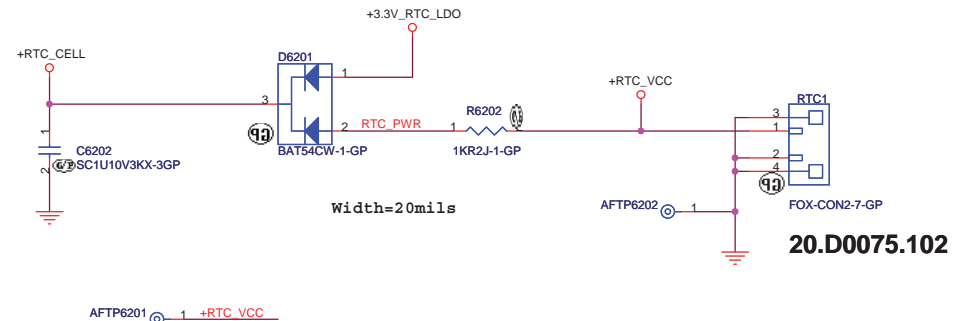
Size
Custom

Document Number
Vostro Calpella

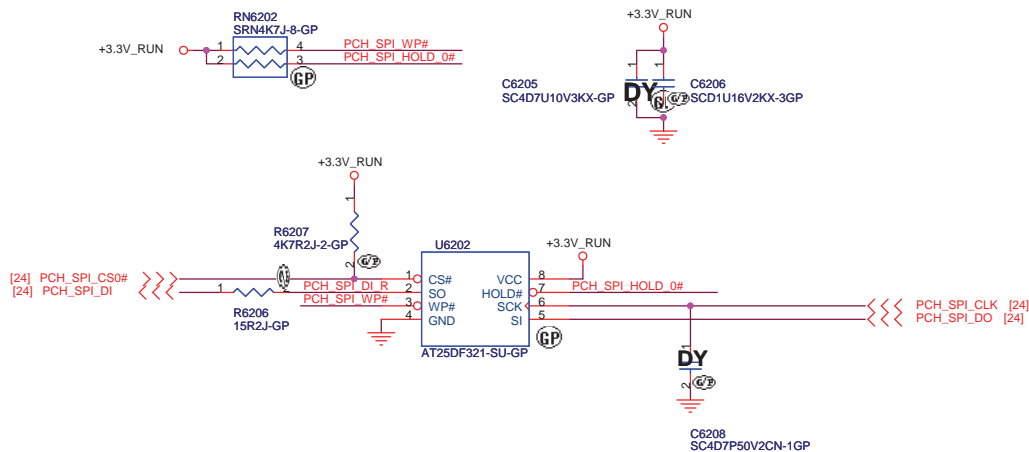
Rev
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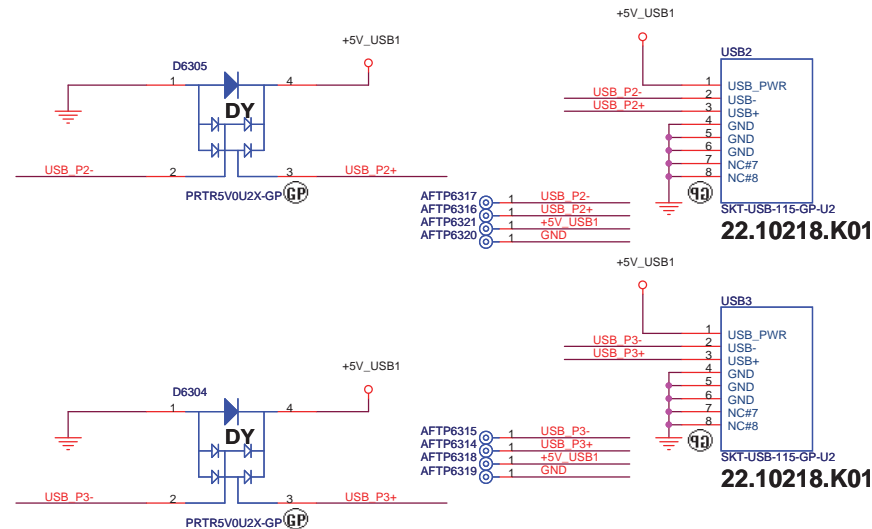
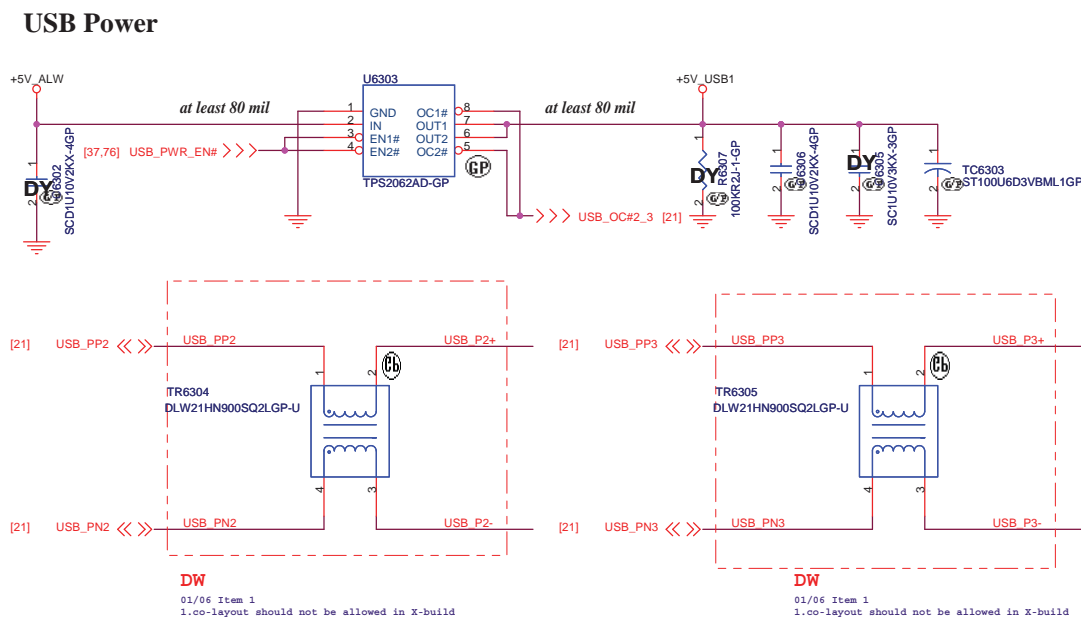
SSID = RBATT



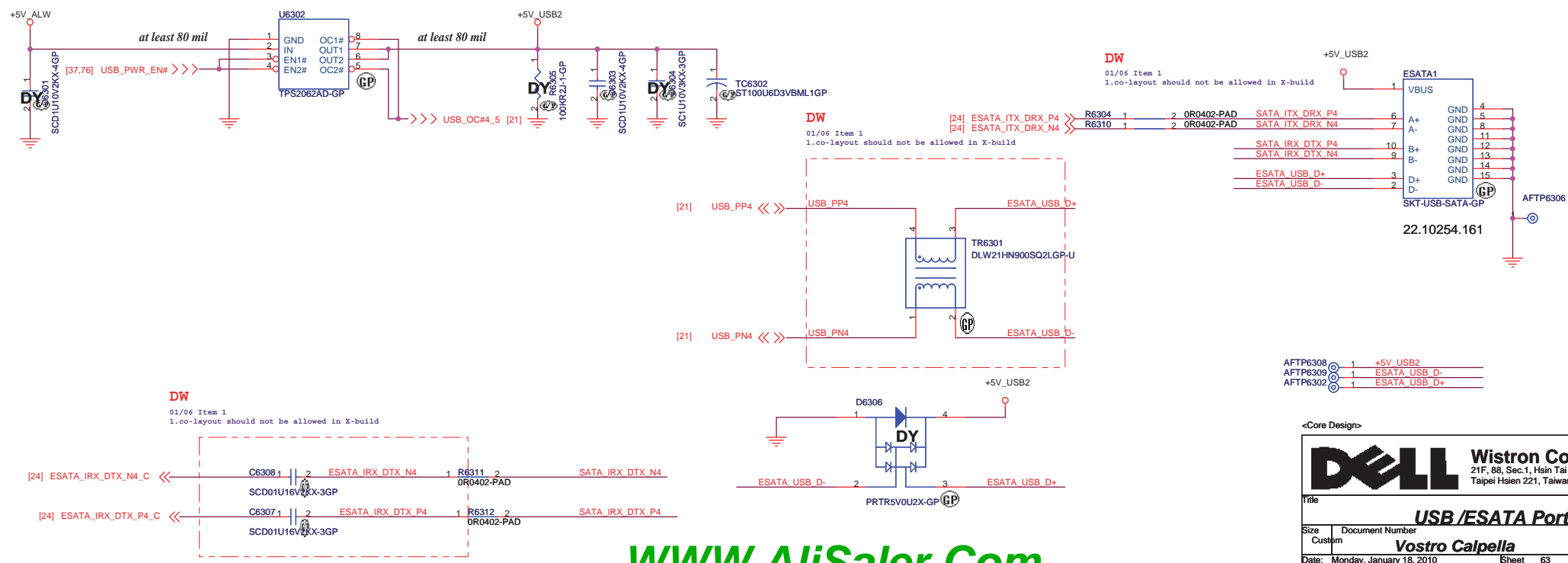
20.D0075.102



USB Power

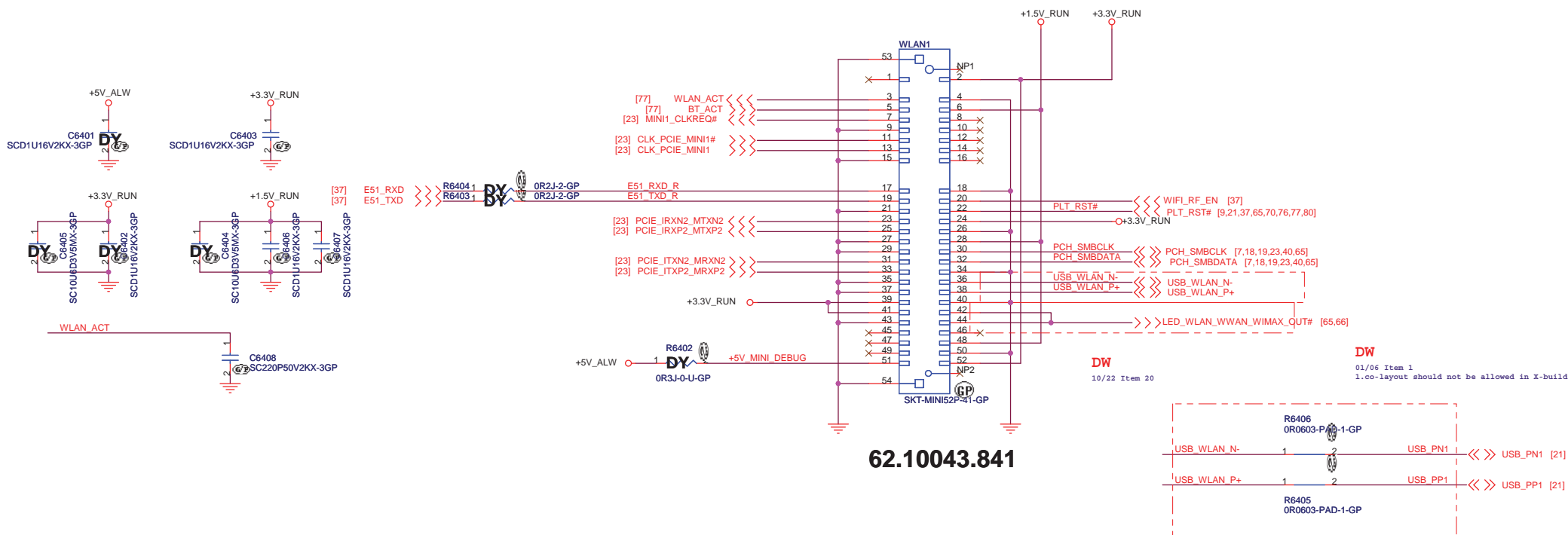


ESATA Power



SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Core Design>



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Title

MINICARD(WLAN)/ITP CONN

Size

Document Number

Rev

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Sheet

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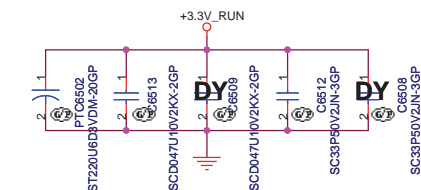
of

91

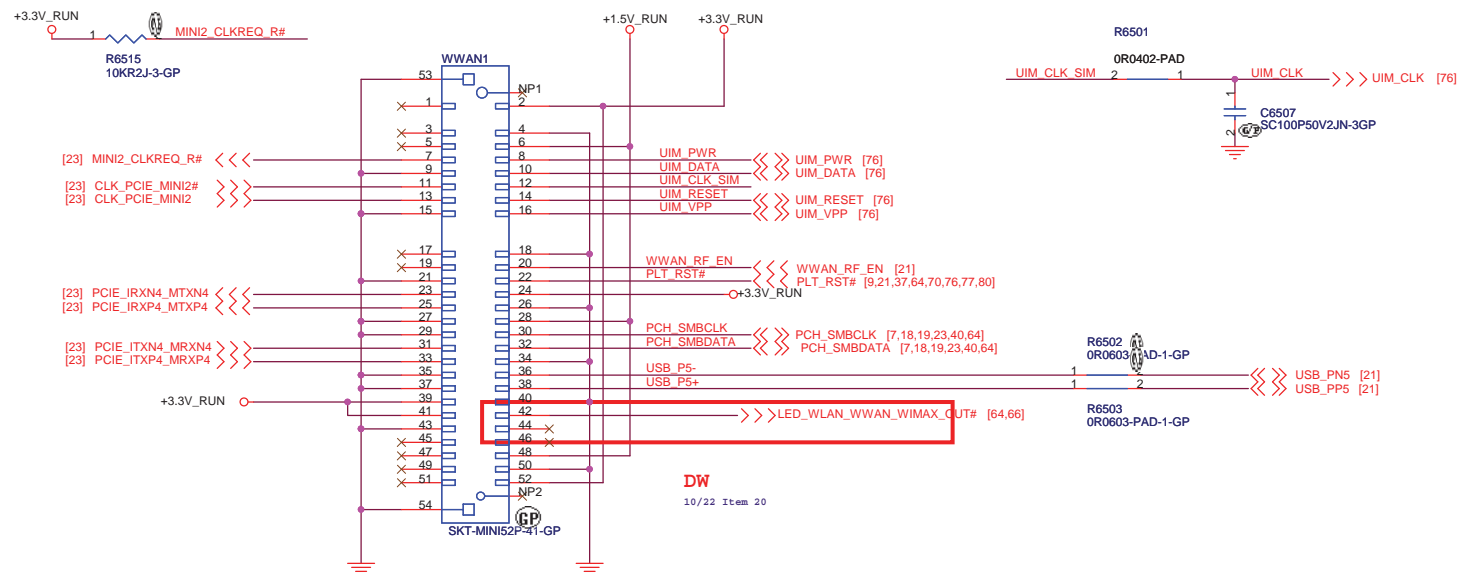
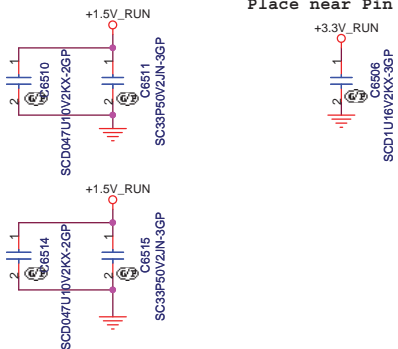
SSID = Wireless

Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



62.10043.841

<Core Design>



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Title

WWAN Connector

Size
A3

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For LED & Capacity board:

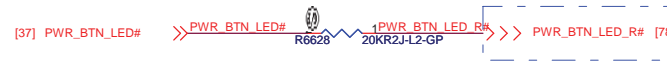
LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WWAN WIMAX LED	White	RUN

For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

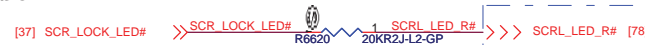
PWR BTN LED

For LED & Capacity board

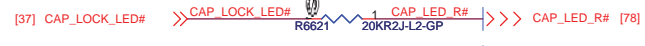


SCRLK LED

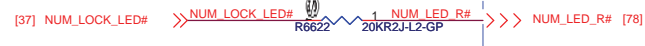
For LED & Capacity board:



CAPS LED



NUM LED



Remove BJT to daughter board

Bluetooth LED

For LED & Capacity board:



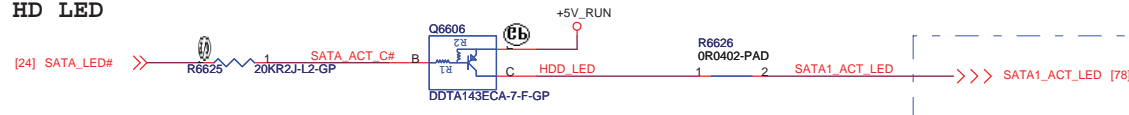
WLAN WWAN WIMAX LED

DW
10/22 Item 20



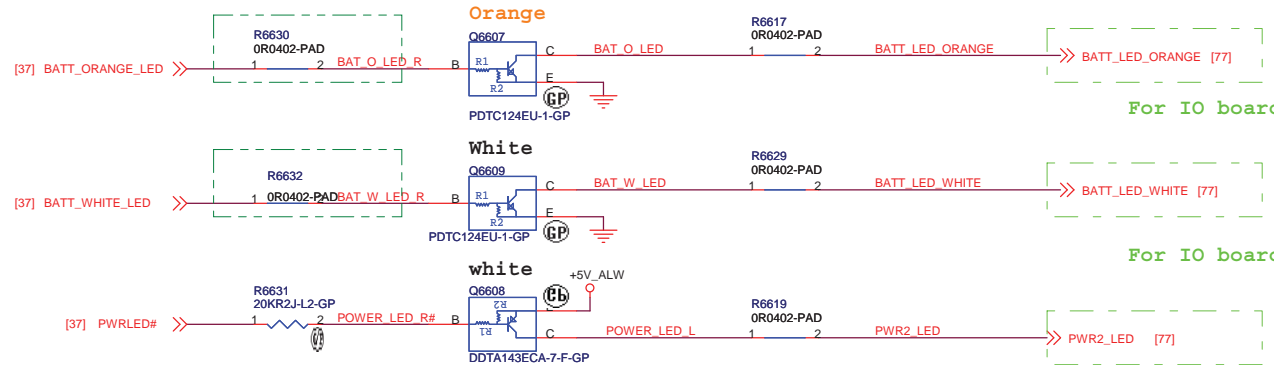
For LED&Capacity board:

HD LED



Battery & Power LED

DW
12/08 Item 5



For IO board

For IO board

For IO board

<Core Design>




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Title		
LED		
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

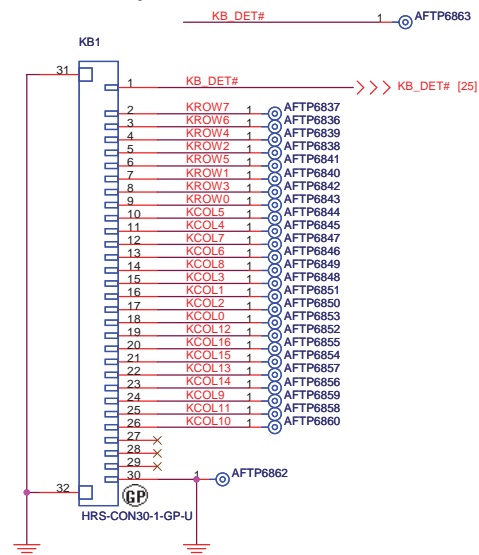
Title

(Reserve)

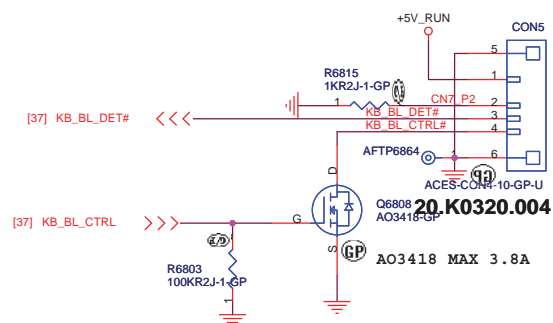
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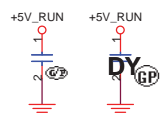
Internal KeyBoard Connector



20.K0259.030

KB Backlight CONN

AFTP6833	1	+5V_RUN
AFTP6832	1	CN7_P2
AFTP6834	1	KB_BL_DET#
AFTP6861	1	KB_BL_CTRL#

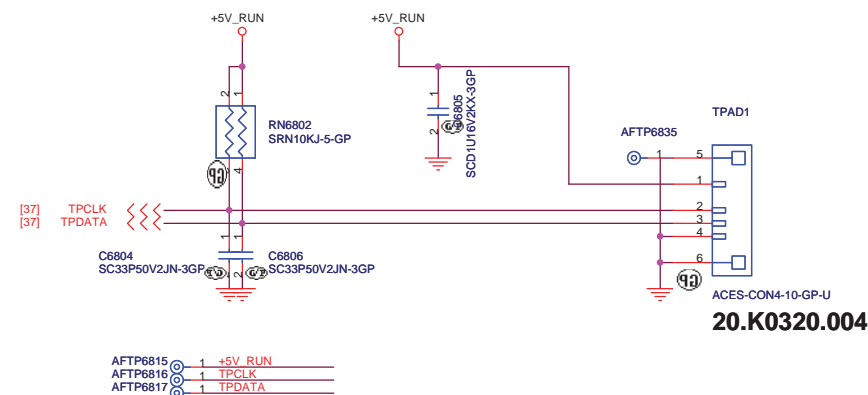


C6812	C6895
SCD1U25V2ZY-1GP	SC4D7U10V5KX-1GP

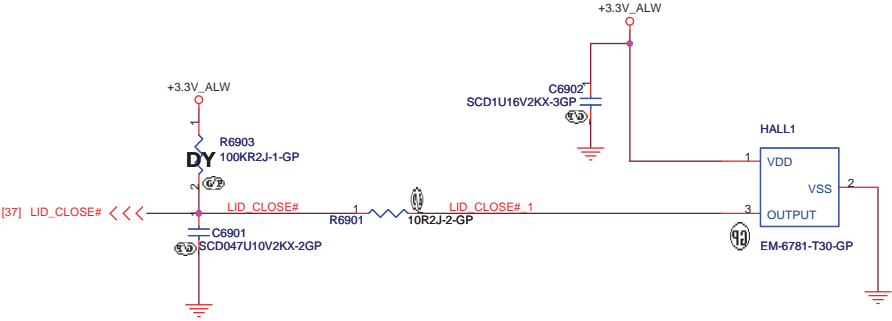
Place near CON5

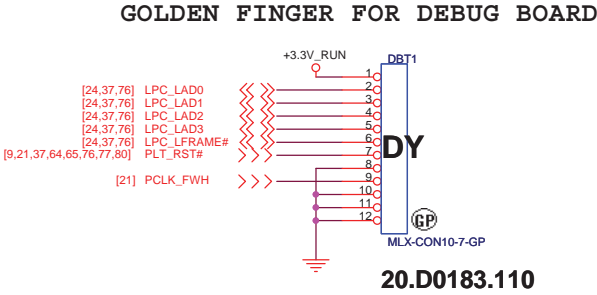
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SSID = Touch.Pad
```

TouchPad Connector



Hall Sensor Connector





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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size

Custom

Document Number

Vostro Calpella

Rev


X01

Date: Monday, January 18, 2010

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<Core Design>



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Title

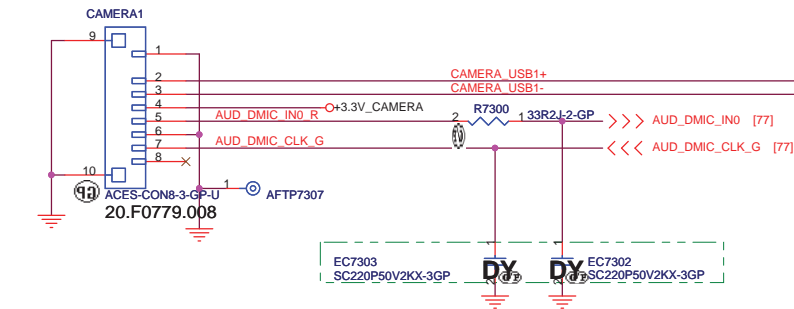
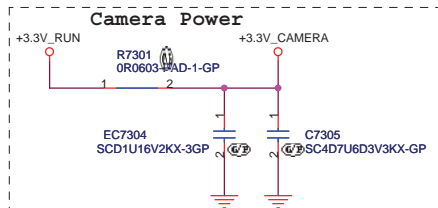
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Size	Document Number	Rev
Custom	Vostro Calpella	X01

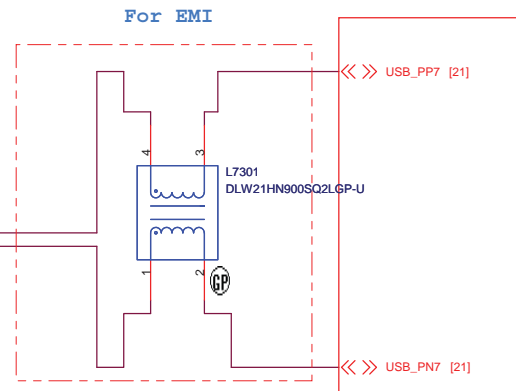
Date: Monday, January 18, 2010	Sheet 72 of 91
--------------------------------	----------------

SSID = User.Interface

Camera Connector



AFTP7303 1 AUD_DMIC_IN0_R
 AFTP7304 1 +3.3V_CAMERA
 AFTP7305 1 CAMERA_USB1-
 AFTP7306 1 CAMERA_USB1+



DW
 01/06 Item 1
 1.co-layout should not be allowed in X-build

DW
 01/18 Item 1

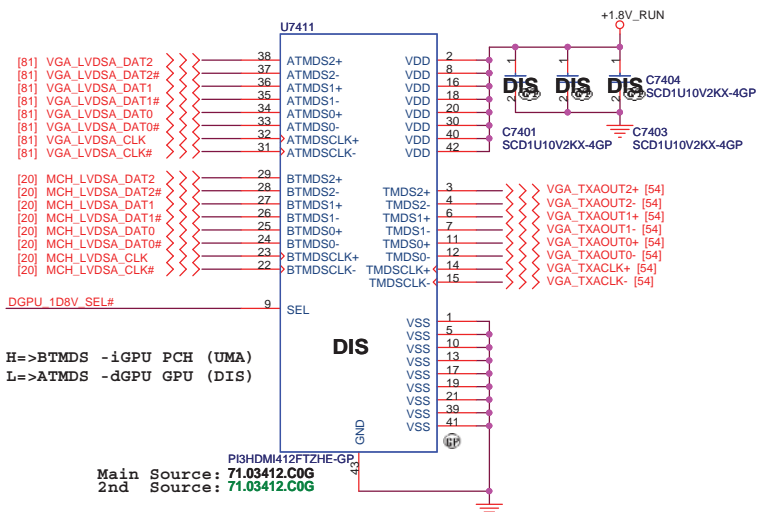
DW
 12/08 Item 5

<Core Design>

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Title			Camera CONN	
Size	Document Number	Rev		
A3	Vostro Montevina Discrete	X01		
Date:	Monday, January 18, 2010	Sheet	73	of 91

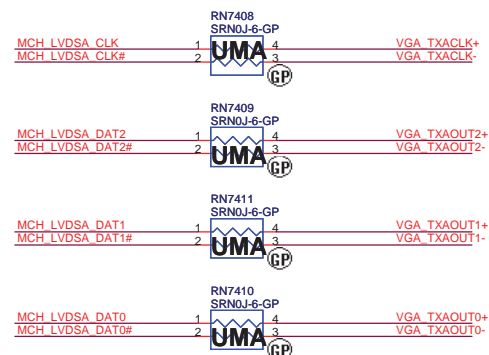
UMA/DIS LVDS signal select circuit



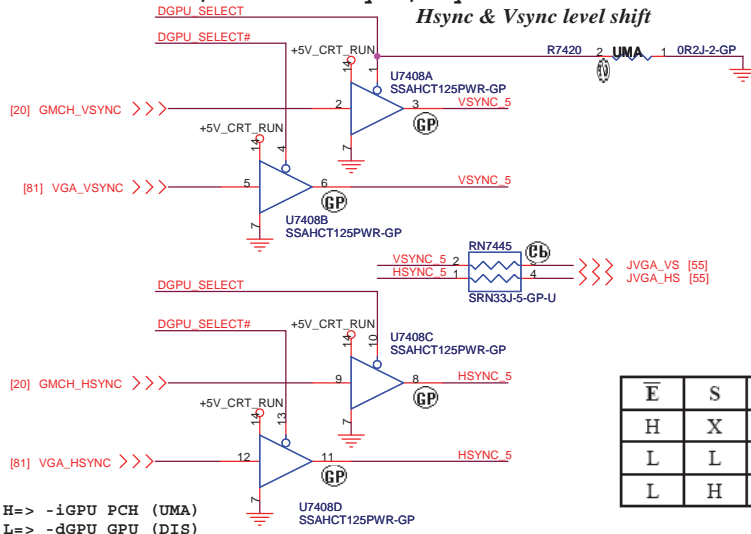
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMSn+ = ATMSn+ TMSn- = ATMSn- TMSCLK+ = ATMSCLK+ TMSCLK- = ATMSCLK- BTMSn+ = High Impedance BTMSn- = High Impedance BTMSCLK+ = High Impedance BTMSCLK- = High Impedance	TMSn+ TMSn- TMSCLK+ TMSCLK-
H	TMSn+ = BTMSn+ TMSn- = BTMSn- TMSCLK+ = BTMSCLK+ TMSCLK- = BTMSCLK- ATMSn+ = High Impedance ATMSn- = High Impedance ATMSCLK+ = High Impedance ATMSCLK- = High Impedance	TMSn+ TMSn- TMSCLK+ TMSCLK-

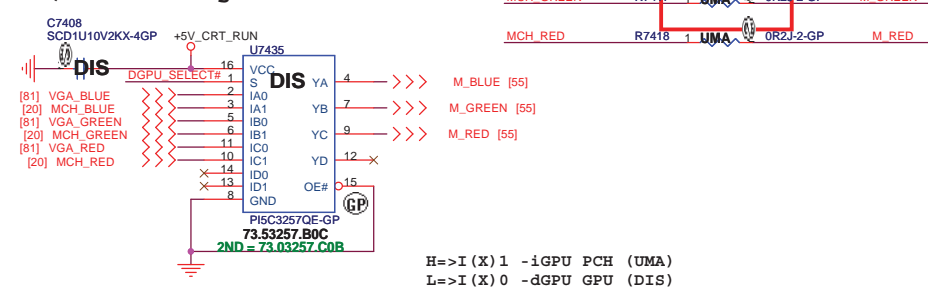
UMA LVDS signal circuit



UMA/DIS CRT Hsync/Vsync select circuit



UMA/DIS CRT signal select circuit



H=>I(X)1 -iGPU PCH (UMA)
L=>I(X)0 -dGPU GPU (DIS)

E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.


File: **Swith-1**

Size: Custom Document Number: **Vostro Calpella** Rev: **X01**

Date: Monday, January 18, 2010 Sheet 74 of 91

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<Core Design>



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Title

Size
A3

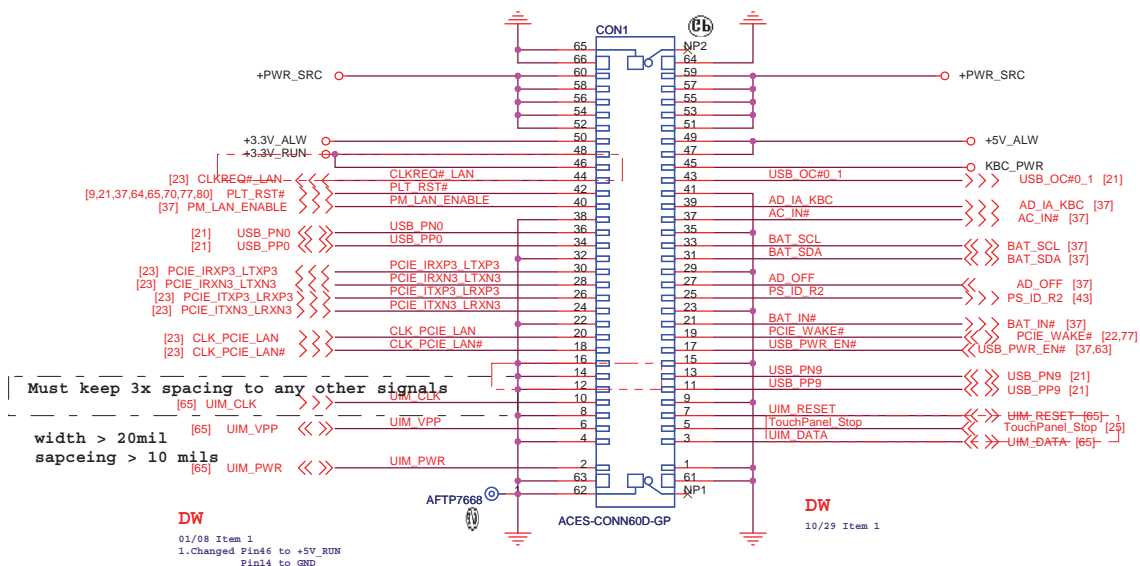
Document Number
Vostro Calpella

Rev
X01

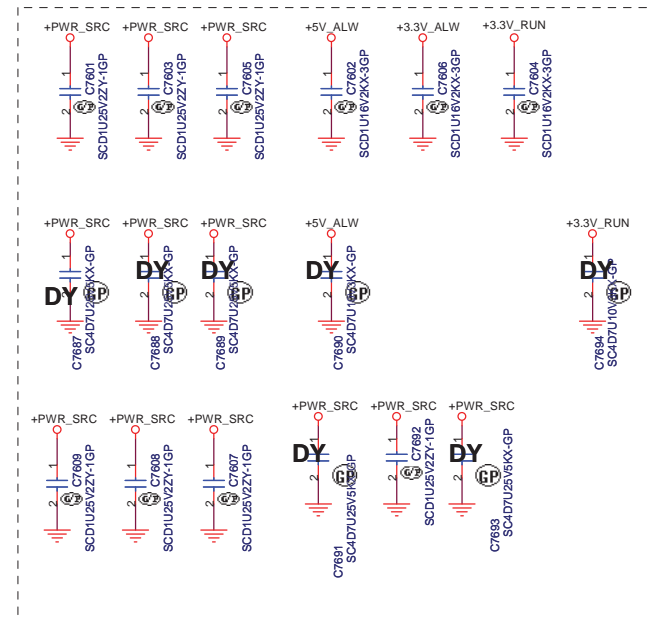
Date: Monday, January 18, 2010

Sheet 75 of 91

DC_IN board CON



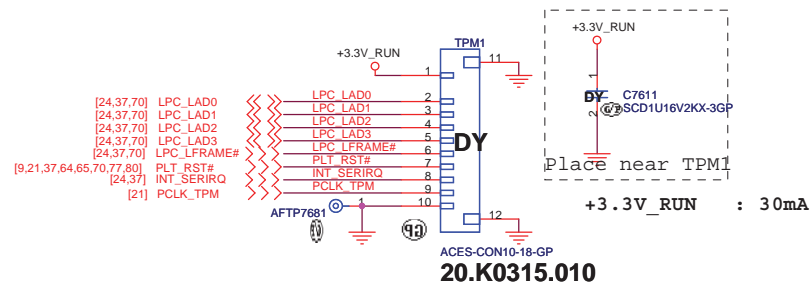
Place near CON1



+5V_ALW : 2000mA
+3.3V_ALW : 347mA
+3.3V_RUN/+5V_RUN:80mA (Touch Panel)
KBC_PWR : < 1mA
+PWR_SRC : Estimated by using battery 11.1V,85W

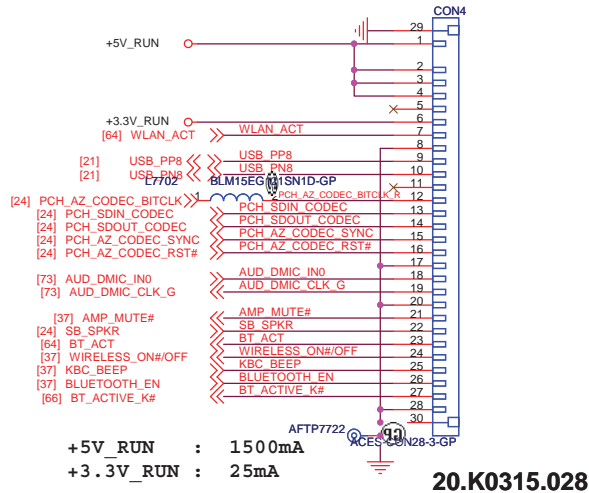
DW
01/08 Item 1
1.Remove DC-IN Board AFTP

TPM board CON

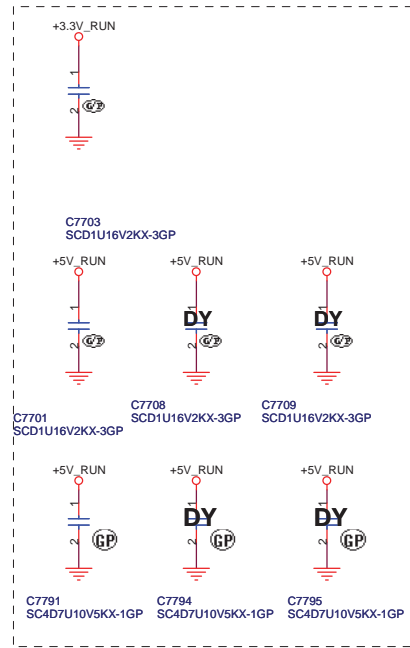


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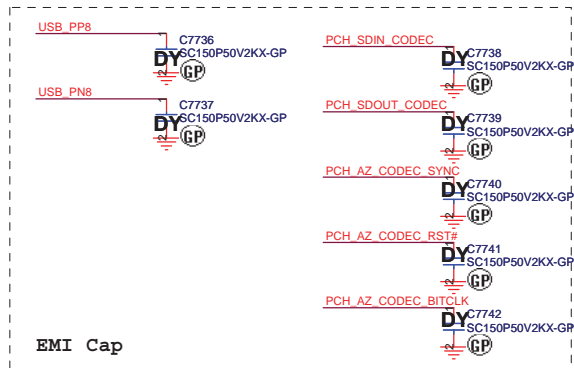
Audio board CON



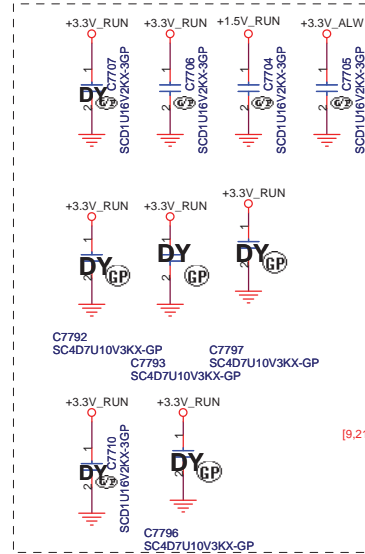
Place near CON4



AFTP7710	1	+5V_RUN
AFTP7706	1	+3.3V_RUN
AFTP7709	1	WIRELESS_ON#OFF
AFTP7702	1	WLAN_ACT
AFTP7703	1	BLUETOOTH_EN
AFTP7704	1	BT_ACTIVE_K#
AFTP7705	1	BT_ACT
AFTP7707	1	USB_PP8
AFTP7708	1	USB_PP8
AFTP7712	1	PCH_AZ_CODEC_BITCLK_R
AFTP7713	1	PCH_SDIN_CODEC
AFTP7714	1	PCH_SDOUT_CODEC
AFTP7715	1	PCH_AZ_CODEC_SYNC
AFTP7716	1	PCH_AZ_CODEC_RST#
AFTP7718	1	SB_SPKR
AFTP7719	1	KBC_BEEP
AFTP7720	1	AUD_DMIC_IN0
AFTP7721	1	AUD_DMIC_CLK_G
AFTP7723	1	AMP_MUTE#

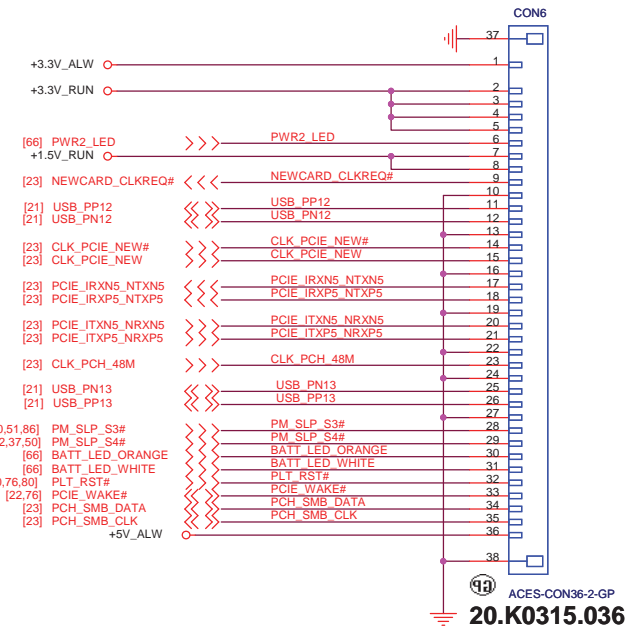


Place near CON6



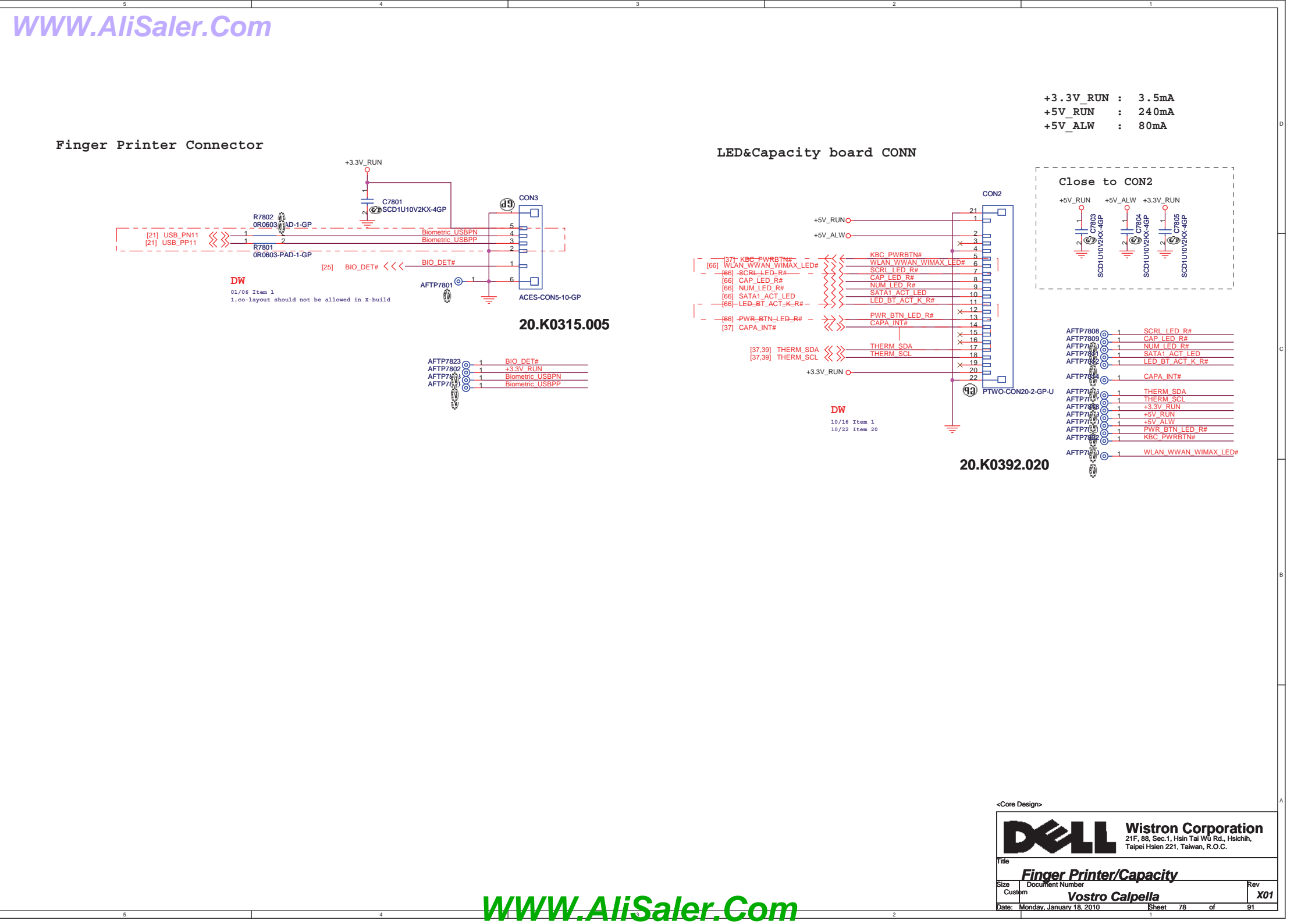
AFTP7758	1	+3.3V_ALW
AFTP7757	1	+3.3V_RUN
AFTP7760	1	+1.5V_RUN
AFTP7762	1	USB_PP12
AFTP7759	1	USB_PP12
AFTP7769	1	NEWCARD_CLKREQ#
AFTP7768	1	PCH_SMB_CLK
AFTP7767	1	PCH_SMB_DATA
AFTP7777	1	PM_SLP_S3#
AFTP7776	1	PM_SLP_S4#
AFTP7773	1	BATT_LED_ORANGE
AFTP7772	1	PWR2_LED
AFTP7781	1	PLT_RST#
AFTP7785	1	BATT_LED_WHITE
AFTP7787	1	+5V_ALW
AFTP7771	1	CLK_PCIE_NEW#
AFTP7770	1	CLK_PCIE_NEW
AFTP7761	1	PCIE_IRXN5_NTXN5
AFTP7765	1	PCIE_IRXP5_NTXP5
AFTP7764	1	PCIE_ITXN5_NRXN5
AFTP7763	1	PCIE_ITXP5_NRXP5
AFTP7775	1	USB_PP13
AFTP7766	1	USB_PP13
AFTP7774	1	PCIE_WAKE#
AFTP7778	1	CLK_PCH_48M

IO board CON



<Core Design>

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Title: Audio BD/IO BD CONN			
Size: Custom	Document Number: Vostro Montevina Discrete	Rev: X01	
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Finger Printer Connector

20.K0315.005

AFTP7823 1 BIO_DET#
AFTP7802 1 +3.3V_RUN
AFTP7801 1 Biometric USBPN
AFTP7800 1 Biometric USBPP

DW
01/06 Item 1
1.co-layout should not be allowed in X-build

LED&Capacity board CONN

20.K0392.020

DW
10/16 Item 1
10/22 Item 20

Close to CON2

+5V_RUN : 3.5mA
+5V_RUN : 240mA
+5V_ALW : 80mA

AFTP7808 1 SCRL_LED_R#
AFTP7809 1 CAP_LED_R#
AFTP7807 1 NUM_LED_R#
AFTP7806 1 SATA1_ACT_LED
AFTP7805 1 LED_BT_ACT_K_R#
AFTP7804 1 CAPA_INT#
AFTP7803 1 THERM_SDA
AFTP7802 1 THERM_SCL
AFTP7801 1 +3.3V_RUN
AFTP7800 1 +5V_ALW
AFTP7799 1 PWR_BTN_LED_R#
AFTP7798 1 KBC_PWRBTN#
AFTP7797 1 WLAN_WWAN_WIMAX_LED#

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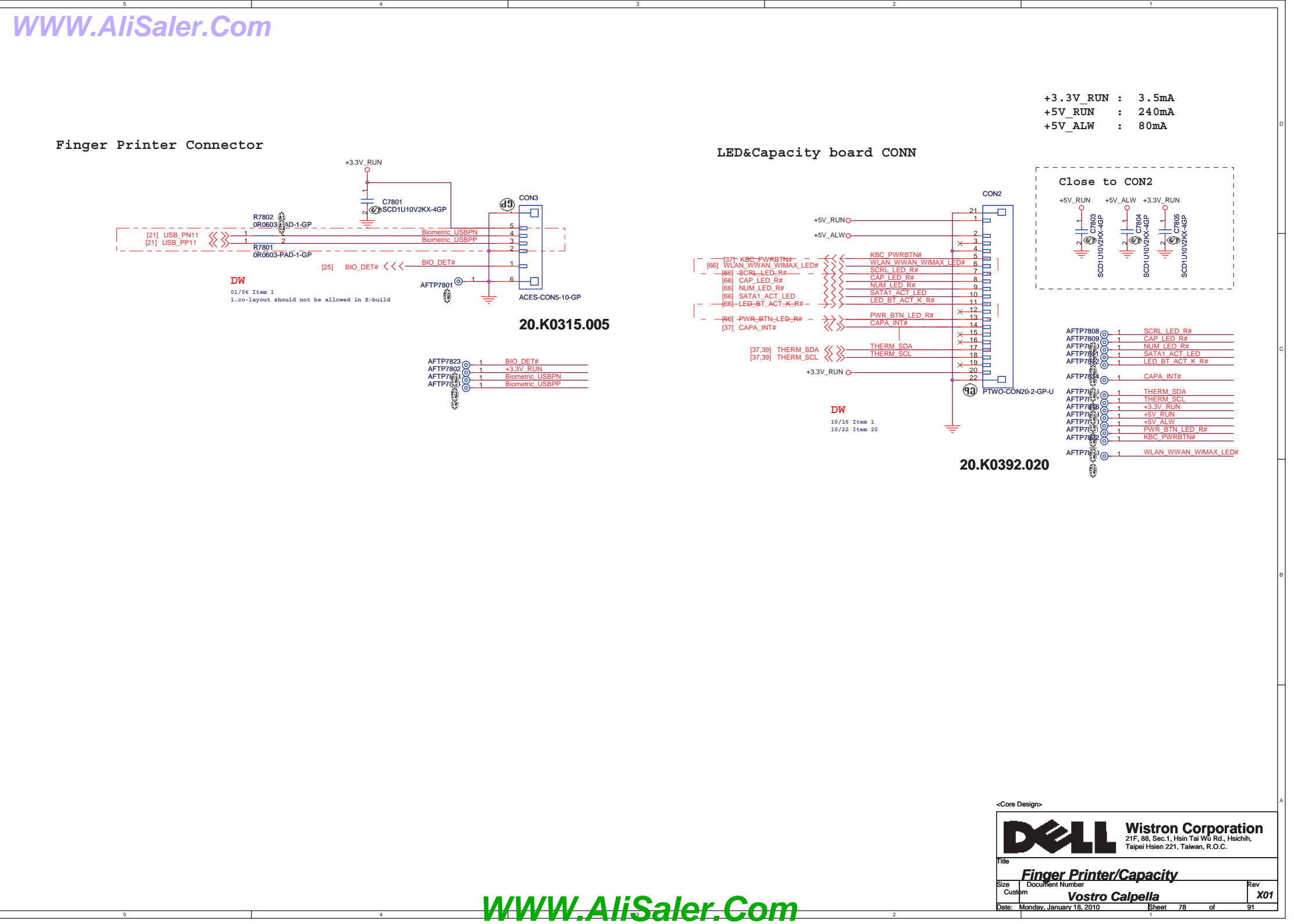
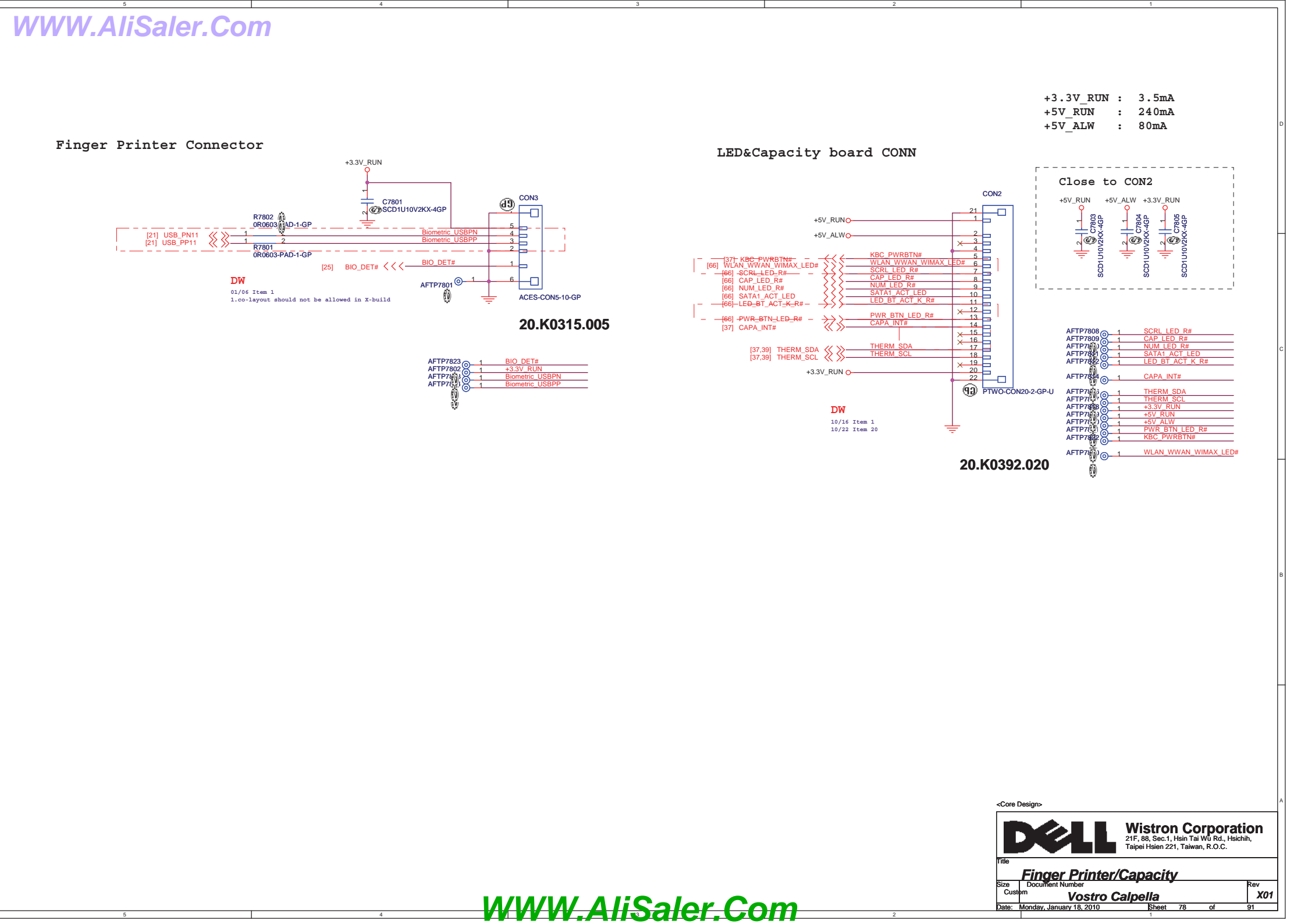
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Title
Finger Printer/Capacity

Size Custom Document Number Vostro Calpella Rev X01

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Finger Printer Connector

20.K0315.005

AFTP7823 1 BIO_DET#
AFTP7802 1 +3.3V_RUN
AFTP7801 1 Biometric USBPN
AFTP7800 1 Biometric USBPP

DW
01/06 Item 1
1.co-layout should not be allowed in X-build

LED&Capacity board CONN

20.K0392.020

DW
10/16 Item 1
10/22 Item 20

Close to CON2

+5V_RUN : 3.5mA
+5V_RUN : 240mA
+5V_ALW : 80mA

AFTP7808 1 SCRL_LED_R#
AFTP7809 1 CAP_LED_R#
AFTP7807 1 NUM_LED_R#
AFTP7806 1 SATA1_ACT_LED
AFTP7805 1 LED_BT_ACT_K_R#
AFTP7804 1 CAPA_INT#
AFTP7803 1 THERM_SDA
AFTP7802 1 THERM_SCL
AFTP7801 1 +3.3V_RUN
AFTP7800 1 +5V_ALW
AFTP7799 1 PWR_BTN_LED_R#
AFTP7798 1 KBC_PWRBTN#
AFTP7797 1 WLAN_WWAN_WIMAX_LED#

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<Core Design>

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Title
Finger Printer/Capacity

Size Custom Document Number Vostro Calpella Rev X01

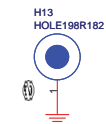
Date: Monday, January 18, 2010 Sheet 78 of 91

DW

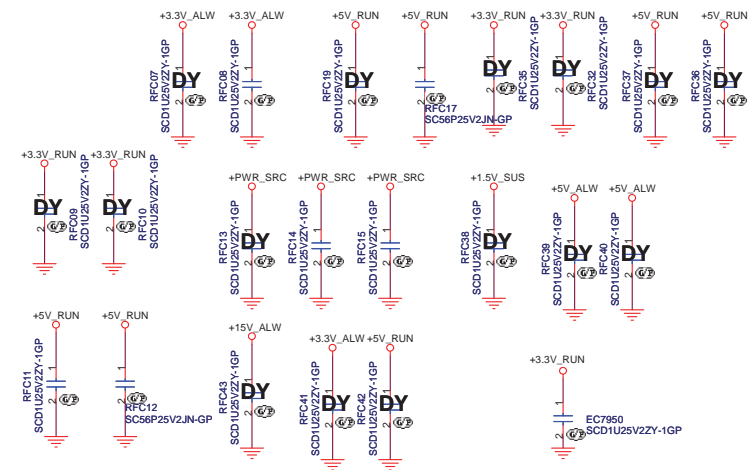


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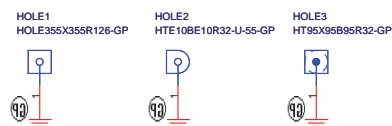
12/03 Item 5



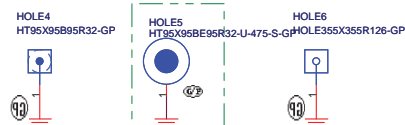
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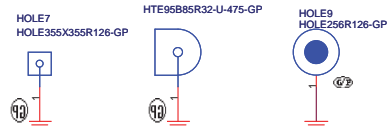
34.4ES31.001 34.4ES31.001



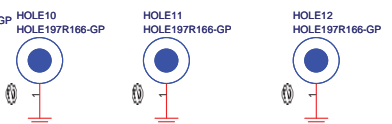
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ZZ.00PAD.N81 ZZ.00PAD.Q41 ZZ.00PAD.I71



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34.4EM01.001 34.4EM01.001 34.4EM01.001

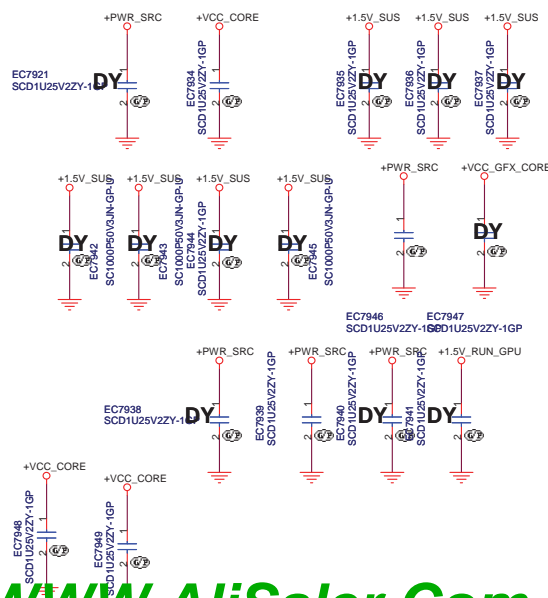
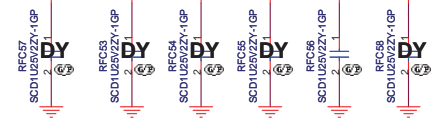
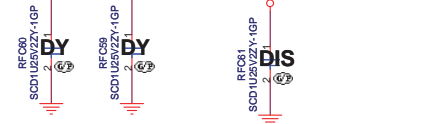


Figure 1 illustrates the test setup for the SCD1U25V22Y-1GP capacitor. The diagram shows six test points (RFC44, RFC46, RFC47, RFC48, RFC49, RFC50) connected to various power and ground rails. Each test point is connected to a 100 pF capacitor (Cp) and a 100 pF capacitor (Cp) in parallel. The power rails are labeled: +PWR_SRC, +VCC_CORE, +1.05V_VTT, and +1.5V_SUS. The ground rails are labeled: SCD1U25V22Y-1GP and SCD1U25V22Y-1GP. The capacitors are labeled: RFC44, RFC46, RFC47, RFC48, RFC49, and RFC50.

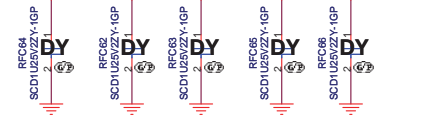
+PWR_SRC +PWR_SRC +PWR_SRC +PWR_SRC +PWR_SRC +PWR_SRC



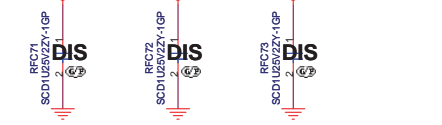
+1.8V_RUN +1.8V_RUN



+5V_ALW +5V_ALW +5V_ALW +3.3V_ALW +3.3V_ALW



+VCC_GFX_CORE +VCC_GFX_CORE +VCC_GFX_CORE



<Core Design>



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Title			
Miscellaneous Components			
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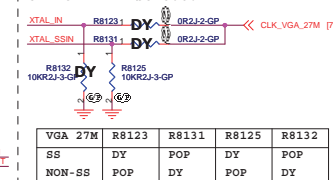
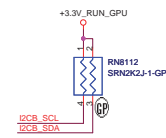
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Size	Document Number	Rev
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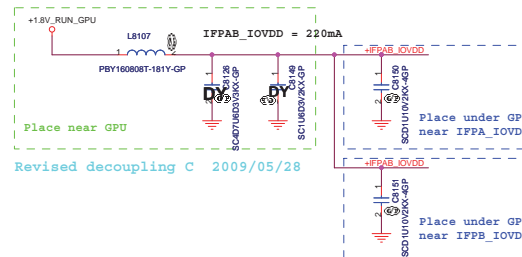
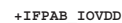
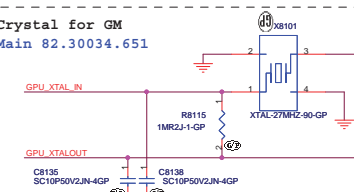
A3	Vostro Calpella	X
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Vostro Calpenna		Sheet 80 of 01	
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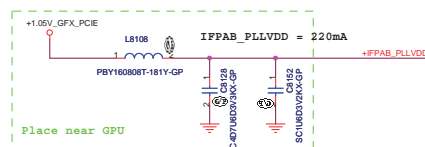


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| | Crystal for GM
| | Main 82.30034.651
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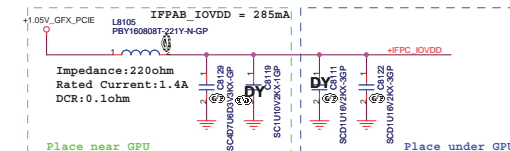


Revised decoupling C 2009/05/28

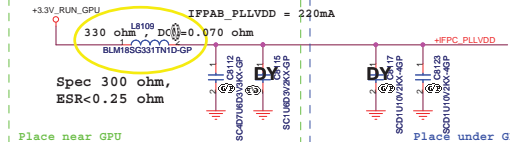
+IFPAB PLLVDD



+IFPC IOVDD

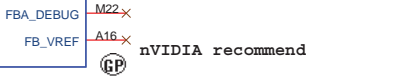
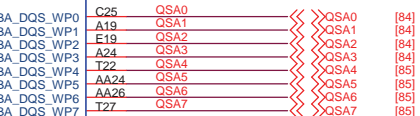
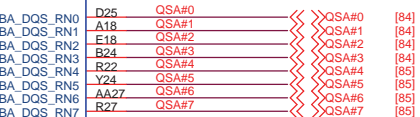
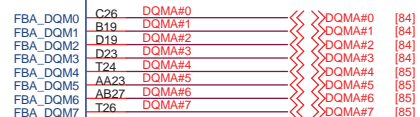
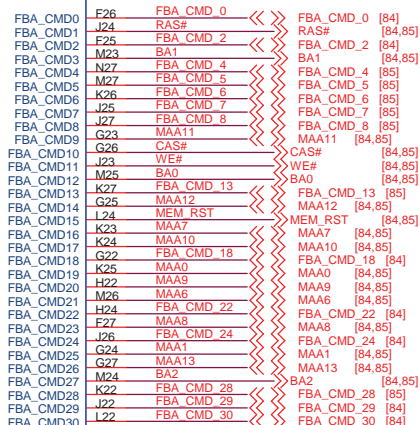
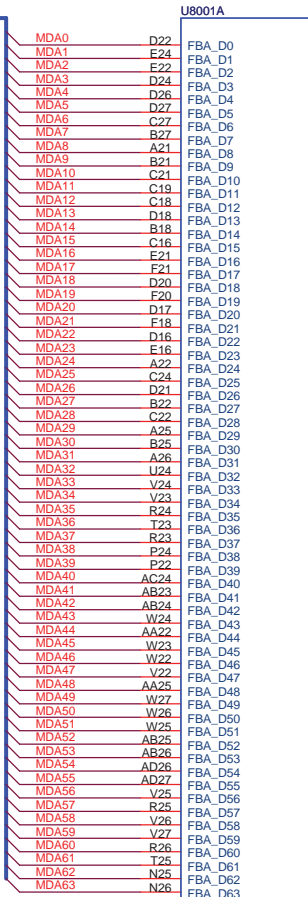


+IFPC PLLVDD

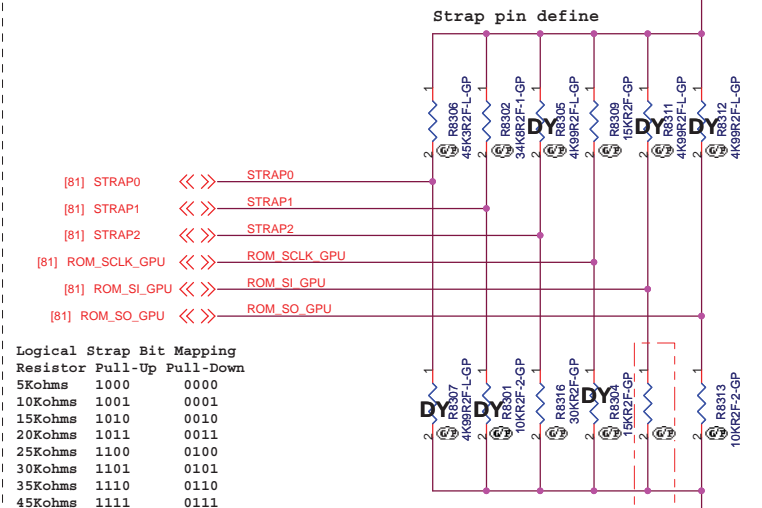


SSID = VIDEO

[84,85] MDA[0..63] <<



Strap pin resistor need use 1% resistor (NV Design Guide)



Strap0 Strap1 Strap2
 USER_BIT0 1 3GIO_PADCFG_LUT_ADR0 0 PCI_DEVID_0 1
 USER_BIT1 1 3GIO_PADCFG_LUT_ADR1 1 PCI_DEVID_1 0
 USER_BIT2 1 3GIO_PADCFG_LUT_ADR2 1 PCI_DEVID_2 1
 USER_BIT3 1 3GIO_PADCFG_LUT_ADR3 1 PCI_DEVID_3 0

EDID is used Reserved N11M-GE1 GPU Device ID=0x0A75

ROM_SI_GPU ROM_SO_GPU ROM_SCLK_GPU
 RAM_CFG0 VGA_DEVICE 1 PEX_PLL_EN_TERM 0
 RAM_CFG1 SMB_ALT_ADDR 0 SLOT_CLK_CONFIG 1
 RAM_CFG2 FB_0_BAR_SIZE 0 SUB_VENDOR 0
 RAM_CFG3 XCLK_417 0 PCI_DEVID_4 1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)

RAM_CFG[3:0] Config FB_BUS Width Definitions
 0000
 0001
 0010 64MX16 DDR3 64Bit Hynix
 0011 04MX16 DDR3 64Bit Samsung Default
 0100
 0101
 0110
 0111
 0111

If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K

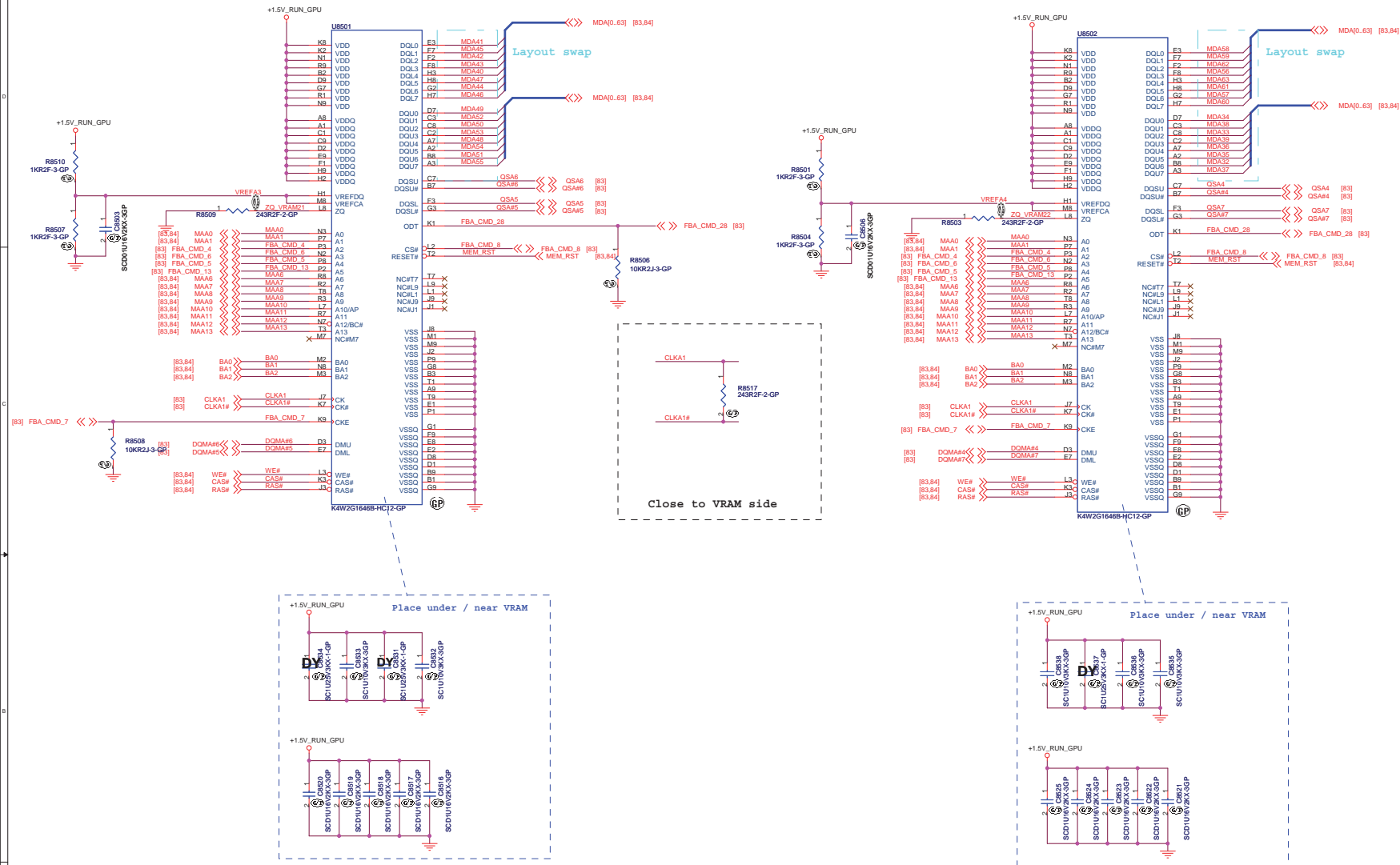
SUB_VENDOR XCLK_417 PEX_PLL_EN_TERM
 0 No VBIOS ROM 0 277MHz(POR) 0 Disable (POR)
 1 BIOS ROM present 1 Reserved 1 Enable

3GIO_PADCFG USER[3:0]
 0000 Desktop 1111 Use EDID to detect panel settings
 1110 Notebook (POR)

SLOT_CLOCK_CFG
 0 GPU and MCH do not share a common reference clock
 1 GPU and MCH share a common reference clock (POR)

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Title
 VGA-MEMORY/STRAPS(4/4)
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<Core Design>

$$V_{out} = 0.704V * (R1 + R2) / R2$$

DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A < OCP < 21.81A

Frequency setting
470K --> 290KHz
200K --> 340KHz
100K --> 380KHz
39K --> 430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
L	H	1.03V
L	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEP5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

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Title			
<i>TPS51218 +VCC GFX CORE</i>			
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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/15	X01	1	25	Swapped Q2515 C,E Pin	For correct.	EE
		2	All	Combine pull-up/down resistors from single to series resistor	For save more part counts	EE
		3	37	Update 10mW circuit.	For DC mode power consumption can be less than 10mW under S5.	EE
		4	22	Add U2213,R2221	Added 3v/5v S5 power good to control resume reset sequence circuit prevent RTC data loss.	EE
		5	51	stuffed PC5105 with 1uF	For power sequencing of +1.8V_RUN , Delay timing	EE
		6	23	Added 25M Crystal	For DCI (DisplayClock_Integration)	EE
		7	79	Added BOSS4	For Steady the thermal module	EE
		9	All	BOSS1 from 34.4W005.001 to 34.4CQ03.101 CON3 from 20.K0315.005 to 20.K0293.006 CON4 from 20.K0315.028 to 20.K0275.028 CON6 from 20.K0315.036 to 20.K0276.036 DM1 from 62.10017.U81 to 62.10017.P31 DM2 from 62.10017.U71 to 62.10017.Q31 HOLE1 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE2 from ZZ.00PAD.K81 to ZZ.00PAD.E11 HOLE3 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE4 from ZZ.00PAD.N81 to ZZ.00PAD.D71 HOLE5 from ZZ.00PAD.K11 to ZZ.00PAD.E11 HOLE6 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE7 from ZZ.00PAD.I71 to ZZ.00PAD.G51 HOLE8 from ZZ.00PAD.N91 to ZZ.00PAD.D31 HOLE9 from ZZ.00PAD.J01 to ZZ.00PAD.D11 LCD1 from 20.F1093.040 to 20.F1555.030 TPAD1 from 20.K0320.004 to 20.K0265.004	For ME request Changed connect PN:	ME
		1	37,87	Removed CAPA_RST# from Capacity board		EE
				Added Switch Baord Detection circuit	For software request.	EE
		1	77	Reversal CON6 Pin 36 <-> 1 ; 35 <-> 2	For new connect pin define.	EE
		2	9,27	Changed RN907,L2701,L2704	For update components	EE
		3	74	Swapped the RN7408,RN7409,RN7410,RN7411	For Layout request.	EE
2009/10/16						
2009/10/19						

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Title			
Change List - EM&RF			
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DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2009/10/22	X011	1	46	PR4604,PR4605 --> 4.7ohm for RT, 0 ohm for TI	Change PU4603 from TPS51125 to RT8205B	Power Team
				PR4622 --> 820k ohm for RT, DY for TI		
				PR4616 --> ASM for RT, DY for TI		
				PR4617 --> DY for RT, ASM for TI		
2009/10/29		53		PC5307 change to 68nF for Intel spec		
		2	50	Add 4.7uF at +PWR_SRC_1D5V	Improve Jitter issue	Power Team

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Title

Change List - Power

Size

Document Number

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